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12TH MICRO/NANO-ELECTRONICS PACKAGING AND ASSEMBLY, DESIGN AND MANUFACTURING FORUM

MiNaPAD Forum 2026

June 3th – 4th

Minatec

Grenoble – France

- **Exhibitions**
- **Conferences**

Organized by IMAPS France – International Microelectronics Assembly and Packaging Society
17 rue de l'Amiral Hamelin – 75016 Paris – France

Wednesday June 3th

8h30 Registration and Welcome to MiNaPAD – Coffee & Soft drink sponsored by

9h00 Opening by Valérie VOLANT (Auditorium)

9h10 Keynote 1 : Corinne Cregut and Emmanuelle Serret, R&D directors, STMicroelectronics, France
IDM End-to-End Co-Optimization of Front-End and Back-End for Robust, Cost-Effective Microelectronics Products

	SESSION A: Dispensing technologies (Auditorium)	SESSION B: Attachment materials (Chrome)
10H00	Real-Time Inline Monitoring of Adhesive Mixing for Process Control in Electronics Packaging (Rose Anne Acedera, Krayden, Philippines)	Development of an electrically conductive, B-stageable adhesive for reliable ceramic MEMS package assembly (Jochen Schuermans, Roartis, France)
10H30	Advances in Sintering Materials for Varying Substrate Sizes "From Slit-Nozzle Dispensing for large substrate area to Jet Dispensing for small diodes (Anne-Marie LAÜGT, Inventec, France)	AI Data Centre ASIC Cooling – Advanced Solder-TIMs (Karthik Vijay, Indium Corporation, United Kingdom)

11h00 – 11h30 Exhibition Opening (Exhibition Hall) / Coffee break sponsored by

	SESSION C: Sustainability (Auditorium)	SESSION D: Sintering materials (Chrome)
11h30	Additive manufacturing fabrication and LCA of PCBs for remote control (Tallal JAMAL, CEA Liten, France and EDMUND WHITMORE, 4MOD Technology, France)	Pressure-less silver sintering for power application: impact of silver, gold or copper surface finishes on microstructure and mechanical performances (M. VELUIRE, UGA / CEA Leti , France)
12h00	Learn about 3D integration through its environmental impact (Mathilde Billaud, CEA Leti, France)	Evaluation of various Cu-sinter materials using different sintering atmospheres and conditions (Simon Merkert, PINK GmbH Thermosysteme, Germany)

12h30 – 13h40 Lunch (Exhibition Hall) sponsored by

13H40 Keynote 2 : Steffen Kröhnert, President & Founder, ESPAT-Consulting, Germany
Electronics Packaging in Europe - Where we are three years after EU Chips Act 1.0

	SESSION E: Packaging Architecture (Auditorium)	SESSION F: Reliability (Chrome)
14h15	Low Profile Waterproof Pressure Sensor (Andrea Ratti, STMicroelectronics, Italy)	Platform for the characterization of electronic components during aging under thermal and electrical stresses (Corentin ROULEAU, Univ de Bordeaux / EDF,France)
14h45	Case studies: applied reliability for European electronics (Maximilian Wallrodt, Micro Systems Engineering GmbH, Germany)	Thermal Cycling Durability Model for Lead-Free Wafer Level Packages Jean-Baptiste Libot, Philippe Milesi, Hooke Electronics, France
15h15	Toward a reproducible fabrication process of a magneto-optic trap for ultra-cold atom sources. (Leopold Boudier, Univ de Toulouse /CNRS-LAAS, France)	Sinter Lamination in Planar Transformer PCB Technology:Reliability Assessment and Path Towards ECSS Standardization for Aerospace Applications (Inge Platteaux, Advanced Circuit Boards (ACB), Belgium)

15h45 – 16H15 Exhibition / Coffee break sponsored by

	SESSION G: Process optimization (Auditorium)	SESSION H: Characterization (Chrome)
16h15	**Optimizing indium bump deoxidation through 3D surface profilometry** (....Chaumy, SET, France)	**Warpage control during assembly process and panel-level RDL formation for heterogeneous integration** (Yoshiki Maruyama, Resonac Corporation, ...)
16h45	**Atmospheric Plasma Processes for Sustainable Oxide Reduction and Adhesion Enhancement in Power Electronics Packaging** (Dhia Bensalem, Plasmatreat GmbH, Steinhagen, Germany)	**Synchrotron X-ray microtomography, an advanced imagi technique to reveal electronic devices packaging and assembly.** (E. Boller, The European Synchrotron / Insidix, France)
17H15	**Die bending methodology to explore Deep Trench Isolation crack initiation risk in Backside Imager Sensors** (Daniel Pascual, ONTOS Equipment Systems, USA)	**Multi-scale micromechanical testing for new Polymer Core Solder Ball interconnection's reliability in operating conditions** (Y. Marthouret, EMSE/ SMS / Physique et Mécanique des Matériaux (PMM))

17h45 – 18h30 Exhibition Hall

18H30 Social Event

Bus transportation: meeting point MINATEC (3 parvis Louis Néel 38000 Grenoble) (To be confirmed)
Departure Time: 18h30 (To be confirmed)

Location: Domaine de Charmeil, 154 Impasse Grande Grange 38210 St Quentin sur Isère
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Thursday June 4th

8h00 - Opening exhibition and conferences – Coffee & Soft drink sponsored by

8h30 Welcome

8h40 Keynote 3 : Jérôme Teysseyre, Co-Founder, NexStage.Ventures, Singapore
Connecting the Dots: From Technical Excellence to Ecosystem Leadership

Session J: 3D advanced (Auditorium)

9h15 Glass 3D structure via FLICE Technology for advance packaging application
(Aziliz Lecomte, Toulouse Univ./ CNRS-LASS, France)

9h45 Build-Up Fan-Out Wafer-Level Packaging with In-Package Fabrication of 3D Integrated Passive Devices Enabled by 3D- RDL and TPVs for RF/mmWave Applications
(Ayad Ghannam, 3DiS Technologies, France)

Session K: Advanced packaging (Chrome)

9h15 Aluminium Filled Through Glass Vias (TGV): From Idea to Applications
(Nils Burmeister, Fraunhofer Institute for Silicon Technology ISIT, Germany)

9h45 New dielectric materials for low temperature hybrid bonding
(Jeanny Maurice, UGA/CEA Leti, France)

10h15 – 10h45 Exhibition & Coffee break (Exhibition Hall) sponsored by

Session L: PCB substrates (Auditorium)

10h45 Substrate Reliability in Practice: Testing Methods and Design Recommendations for IC Packaging
(David Capeder, Dyconex AG, Switzerland)

11h15 Pioneering Bottom-Up Copper Plating: Advanced Pillar-Like Metallization for High Aspect Ratio Through Glass Vias
(Saminda Dharmarathna, MacdermidAlpha Electronics Solutions, ….)

11h45 Application of Glass Core Substrates for Chiplet Systems
(Claudia Landstorfer, Fraunhofer IZM, Germany)

Session M: Interconnections (Chrome)

10h45 Innovative Pressureless Wire Bonding for High-Power Systems
(Matthias Fettke, PacTech - Packaging Technologies GmbH,Germany)

11h15 Ultra-Precise Dispensing for Advanced Microelectronics Packaging: Materials Versatility and Long-Term Process Stability
(Aneta Wiatrowska, XTPL SA, Poland)

11h45 Investigation of wafer level downscaling challenges in electroplated lead-free microbumps for ultra-fine pitch interconnects
(Stelliane Grolier-Lee, CEA Leti, France)

12h15 – 13h15 Lunch & Exhibition (Exhibition Hall) sponsored by

Session N: Fan-Out (Auditorium)

13h15 Fan Out Wafer Level Packaging – European Manufacturing for Small to Mid-volumes
(Marc Dreissigacker, AEMtec GmbH, Germany)

13h45 Radar with Integrated Antennas based on Fan-Out Wafer-Level Packaging RDL-First Integration
(Arnaud Garnier, CEA Leti, France)

Session O: Flip-Chip (Chrome)

13h15 Underfill adhesive: Thermomechanical and Thermal Storage Optimization
(Oumar N'DIAYE,PROTAVIC INTERNATIONAL, France)

13h45 Sub micron placement accuracy – the era for heterogeneous integration and optoelectronic assemblies(Jonathan Abdilla, BESI Austria GmbH/BESI Switzerland AG)

14h15 – 14h30 Short Break

Session P: Heterogeneous Integration (Auditorium)

14h30 **Packaging and assembly challenges in Photovoltaic (PV) modules: Focus on numerical simulation of the delamination behavior of PV assembly**
(Bertrand Chambion, UGA/CEA Liten, France)

15h00 **Innovative Power Package Solutions for AI GPU Accelerators: UTAC's Two-sided Cooling SPS, High Thermal EMC, and SiP Power Module Advancements**
(Michael Choi, UTAC Group, CA/USA)

15h30 **Innovative assembly and test developments for next gen power and RF semiconductors**
(Ruud de Wit, CITC/TNO, Germany)

16h00 **Closing MiNaPAD 2026 Conference by Valérie VOLANT (Auditorium)**

Address:
Maison MINATEC
3 parvis Louis Néel
38000 Grenoble
centredecongres-maisonminatec@cea.fr

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