EMPC2025

The 25th European Microelectronics & Packaging Conference and Exhibition

OFFICIAL CATALOGUE

15-18 September 2025

Grenoble – France

www.empc2025.org

Co-Sponsor by: IEEE, IEEE Electronics Packaging Society

Organized by: iMAPS Europe

Sponsors: ASE, set, DELO Industrial Adhesives, ST life.augmented, electronmec, YOLE Group

12TH MICRO/NANO-ELECTRONICS PACKAGING AND ASSEMBLY, DESIGN AND MANUFACTURING FORUM

MiNaPAD Forum 2026

June 3th – 4th

Minatec

Grenoble – France

- Exhibitions
- Conferences

Organized by IMAPS France – International Microelectronics Assembly and Packaging Society
17 rue de l'Amiral Hamelin – 75016 Paris – France
+33 (0)7 88 75 59 86 – imaps.france@orange.fr – www.france.imapseurope.org

Summary

IMAPS Europe
Who We Are...

The International Microelectronics and Packaging Society (IMAPS) is the largest society dedicated to the advancement and growth of microelectronics and electronics packaging technologies through professional education and training, interaction with industry and networking amongst professionals and academics. Founded in 1967 as ISHM, IMAPS has professional members in 23 North American chapters and 21 international chapters.

From the founding of ISHM in the 1960s to its evolution into IMAPS today, the Microelectronics and Photonics community has enjoyed and benefited from the global involvement of internationals over the decades.

IMAPS Europe has friendships with IMAPS organisations around the world. Amongst these are close cordial contacts and conversations with our colleagues in Japan, Taiwan and North America.

IMAPS Europe comprises 13 independent local IMAPS Chapters that embrace the community of microelectronics packaging engineers throughout Europe. Their members number over 1500 individuals plus additional corporate members in some chapters. Membership is always local to a chapter. IMAPS Iberia is the newest chapter to join the IMAPS Europe community.

The IMAPS European chapters organize national and international seminars, workshops and conferences, the flagship event being the EMPC, which is held every odd year interleaved with ESTC every even year with mutual access to both events.

EMPC is planned to be held every 3rd week of September in 2025, 2027, 2029, ongoing.

Welcome to the EMPC 2025
Conference in Grenoble, France

World Trade Center Grenoble – 5-7 place Robert Schuman – 38025 Grenoble

After more than a decade, EMPC returns to Grenoble—the heart of the French Alps and a global hub for semiconductor innovation. Following the successful editions of EMPC 2013 and ESTC 2016, we are proud to host the 2025 European Microelectronics and Packaging Conference in this vibrant city once again.

Our previous edition in Cambridge, UK, in 2023 was a resounding success. Building on that momentum, IMAPS Europe has once again entrusted IMAPS France with organizing this prestigious event. Grenoble was the natural choice: home to a robust semiconductor ecosystem including global leaders like STMicroelectronics, Soitec, Aledia, and Kalray; the renowned research institute CEA-LETI; and top-tier universities and engineering schools. For over 15 years, IMAPS France has also hosted the annual MiNaPAD conference here, reinforcing Grenoble's reputation as a center of excellence in microelectronics.

To ensure EMPC 2025 is truly international in scope and spirit, we assembled a diverse team of seasoned organizers and scientific experts. I am especially grateful to Professor Stoyan Stoyanov from the University of Greenwich, who took on the demanding role of Program Chair. Under his leadership, our program committee reviewed over 130 abstract submissions, resulting in one of the most comprehensive and dynamic programs in EMPC history.

This year's conference features seven keynote addresses from distinguished voices across research institutions and industry—ranging from global corporations to agile startups—offering a wide spectrum of insights into the challenges and opportunities shaping our field. These plenary sessions will be complemented by four parallel technical tracks, ensuring a rich and engaging experience for all attendees.

Our exhibition hall sold out nine months in advance—a testament to the enthusiasm and support of our industry partners. Attendees will enjoy the best of French hospitality, with local cuisine and wines served throughout the exhibition space, creating a warm and convivial setting for networking and collaboration.

We extend our heartfelt thanks to our gold sponsor ASE Group, our sponsors STMicroelectronics, SET, Delo, and Electron-mec, and our media partner Yole Group. We are also deeply grateful to the volunteer instructors leading our Professional Development Courses on the opening day. This event would not be possible without the dedication and contributions of so many.

Europe continues to play a vital role in the global technology landscape, and EMPC 2025 is a celebration of our shared commitment to innovation, excellence, and collaboration. Whether you are here to exchange technical knowledge, explore new partnerships, or drive business development, we believe EMPC offers something valuable for everyone.

We are delighted to welcome you to Grenoble, and we wish you an inspiring and productive conference week!

Warm regards,

Jean-Marc Yannou
Chairman, EMPC 2025

General Information

The registration Desk of EMPC 2025 is located in the WTC at the 1er level.
Address :
5—7 place Robert Schuman, BP 1521,
38025 Grenoble, France

▸ Opening Hours

09/15	8:30am – 6:00pm
09/16 – 09/18	8:30am – 6:30pm

▸ Badges
Participants are obliged to wear the official conference badge on all occasions.

▸ Language
The official language of EMPC 2025 is English.

▸ Coffee and lunch
Coffee and Lunch will be served in the exhibitor area only during the breaks between sessions. Lunch will be served in the exhibition hall.

▸ WIFI
Network name: ESPACE-CONGRES
User name EMPC2025
Password: 4xt62nWJ

▸ Disabled persons
Participants with disabilities are kindly requested to contact the congress organizers for assistance when entering the WTC.

▸ Non-smoking Policy
EMPC 2025 will be a non-smoking conference. Smoking is prohibited in all meeting rooms & exhibition of the WTC.

▸ Liability
In participant in EMPC 2025, both participants and exhibitors agree that neither the EMPC 2025 committee nor the Organizing secretariat assume any liability whatever. Participants and sponsors should organize their own health, travel and personal insurance.

Registration Fees

Conference ticket for authors **	550 €
Conference ticket for IMAPS/ IEEE member	770 €
Conference ticket for regular attendees	880 €
Conference ticket for sponsors	550 €
Conference ticket for students ***	200 €
Conference ticket for additional exhibitors	660 €
Professional Development Course (half-day)	200 €
Professional Development Course (full day)	400 €

The prices are net amounts. Companies outside France are not subject to VAT. French companies have to pay 20 % VAT.

Fees cover access to all sessions, the exhibition, the welcome reception, the conference dinner (except for students) and the conference proceedings.

** For every accepted paper one person from the group of authors will have to register at the author rate.

*** The student fee is available for Bachelor and Master students.

Notes

In Memory of Professor Francis Nihal Sinnadurai

Known to all as Nihal

Fellow IEEE, Fellow Institute of Physics, PhD, MSc, BSc, CEng

25 September 1941 – 4 July 2025

It is with deep sorrow that we share the passing of Professor Francis Nihal Sinnadurai - known to all simply as Nihal - a beloved husband, father, grandfather, mentor, and friend.

Born in Colombo, Sri Lanka, Nihal's life was shaped early by both personal loss and inspiration. After the untimely death of his father when Nihal was age three, he was raised by his mother, a hospital Operating Theatre Sister. He showed remarkable academic aptitude and sporting talent from a young age, excelling in cricket and local games. After his family moved to London when he was 15, he achieved extraordinary academic results - even scoring 120% in his A-level Physics and Maths exams, gaining bonus marks for his outstanding performance.

Pioneering Contributions & Recognition

Nihal pursued a parallel career in industry and academia, studying part-time while working, and eventually earning degrees in Physics and Semiconductor Devices from the University of London, followed by a PhD from the University of Southampton. His technical work left a lasting legacy in electronics and microelectronics - from pioneering the adoption of plastic encapsulated microelectronics in high-reliability systems, to inventing the Highly Accelerated Stress Test (HAST) methodology, and contributing fundamentally to liquid crystal micro-thermography.

Though these contributions alone were groundbreaking, Nihal's professional legacy extends far beyond them. He authored over 90 scientific papers, lectured internationally, and served as an expert witness in landmark cases. Over his long career, he became not only a Chartered Engineer but also a respected Fellow of both the IEEE and the Institute of Physics. He held senior roles at British Telecommunications (BT), led private companies, consulted for international organisations including the UNDP and ITU, and mentored generations of engineers.

Nihal received numerous professional awards, including the IMAPS Daniel C Hughes Jr Memorial Award (the first ever awarded to a non-US member), the IMAPS President's Award, and multiple IEEE distinctions, including the Reliability Society Lifetime Achievement Award and Region 8 Volunteer Award. Yet despite these accolades, Nihal remained grounded, driven by a deep sense of ethics and service.

Nihal's lasting impact on IMAPS and the EMPC Conference

But perhaps nowhere was Nihal's influence more deeply felt than in the global microelectronics community - particularly within IMAPS (International Microelectronics Assembly and Packaging Society) and the EMPC

(European Microelectronics and Packaging Conference).

His commitment to IMAPS spanned decades, beginning with local activities in the United Kingdom and evolving into prominent leadership at the European and global levels. As Chair of IMAPS-UK (2001–2003), President of IMAPS Europe (2009–2011), and longtime Secretary of the European Liaison Council (ELC), Nihal helped shape the future of the organisation and its global relevance. He represented European IMAPS chapters with passion and diplomacy, forging strong partnerships across North America, Asia, and beyond.

Nihal played a key role in organising and advancing EMPC, the biennial flagship conference of IMAPS Europe. Whether as organiser, committee member, or mentor to presenters, he was a constant, guiding presence. His work helped strengthen the scientific quality, international participation, and collaborative spirit of EMPC for more than two decades.

Colleagues across the IMAPS community remember him for far more than his official roles. Nihal was a bridge-builder — connecting local chapters, mentoring young professionals, and fostering an open, inclusive spirit of community. His friendship, generosity, and kindness enriched every gathering.

A Life well Lived

Outside of work, Nihal lived with joyful intensity. He completed three marathons, was a keen scuba diver, an avid chess and bridge player, and an environmentalist who planted thousands of trees near his home in Suffolk. "It was through scuba diving that he met his beloved wife, Sara. Sara was also a frequent presence at IMAPS events and has become a good friend to many in the community.

Nihal's legacy reflects a renaissance man: unwaveringly committed to his field, passionate about his interests, and deeply invested in the well-being of his family and friends. He was married 3 times and had 2 children and 5 grandchildren, all now adults. Sara was his third wife, and they enjoyed 21 years of complete happiness together and strong mutual support until his death."

As we remember Nihal, we celebrate not only his monumental achievements but also the joy, intellect, and humanity he brought into the lives of so many. His memory will live on in his contributions to science, his love for life, and the countless hearts he touched along the way.

Our thoughts are with his beloved wife Sara, his children, and grandchildren.
He will be deeply missed, but never forgotten.

Sponsors Information

ASE, Inc. is the leading global provider of semiconductor manufacturing services in assembly and test. In a world that runs on semiconductor technology to achieve lifestyle, efficiency and sustainability goals, packaging innovation is at the heart of what ASE does. Today, ASE is delivering on the promise of heterogeneous integration, through advanced packaging, system-in-package, and chiplet solutions to meet growth momentum across HPC, Automotive, AI, 5G, and more.

SET (Smart Equipment Technology) is a world-leading supplier of high-accuracy Flip-Chip Bonders and versatile Nanoimprint Lithography (NIL) solutions. Since 1975, we have designed and manufactured leading-edge semiconductor equipment for high-precision applications.
We support laboratories and semiconductor companies seeking world-class precision and superlative reliability in the assembly of their components. With our Flip-Chip Bonders installed worldwide, SET's equipment is globally renowned for unsurpassed sub-micron accuracy and incomparable flexibility.
Ranging from manual-loading to fully-automated solutions, our Flip-Chip Bonders cover a wide range of bonding applications and possess the unique ability to handle and bond fragile and/or small components onto substrates up to 300 mm.

DELO is a leading manufacturer of high-tech adhesives and other multifunctional materials as well as adhesive dispensing and curing technology. Its products are mainly used in the semiconductor, automotive, and consumer electronics industries. They can be found in almost every mobile phone and in most cars worldwide, for example in cameras, loudspeakers, electric motors, or sensors. Customers include Bosch, Huawei, Mercedes-Benz, Osram, Siemens, and Sony. DELO's headquarters are in Windach, Germany, near Munich, with subsidiaries in China, Japan, Malaysia, Singapore, and USA, as well as representative offices and distributors in numerous other countries.

Electron Mec is committed to providing world best in class tools, processes and services to High-Tech players in Europe, meeting and exceeding the requirements of its customers. Based in France, Italy, Germany, Switzerland and Spain we support our partners locally relying on process knowledge and experience

STMicroelectronics (ST) is a global semiconductor leader, delivering innovative and sustainable solutions that are at the forefront of enabling smarter and more connected technologies. With a rich history spanning over three decades, ST combines cutting-edge expertise with a commitment to sustainability, empowering industries and individuals to address the challenges of today and shape a better tomorrow.

ST operates at the heart of diverse technological advancements, offering a comprehensive portfolio of products and solutions that serve key markets such as automotive, industrial, personal electronics, communications equipment, and the Internet of Things (IoT). Our technologies are designed to drive progress in areas such as:

- Smart mobility, advanced electric vehicles, autonomous driving, and connected cars
- Power and energy management, enabling energy-efficient systems and renewable energy solutions
- IoT and connectivity, fostering the seamless integration of devices and ecosystems
- Artificial intelligence at the edge, bringing intelligence closer to where data is generated

With a global presence in 35 countries, 14 manufacturing sites, and 80 sales offices, ST is uniquely positioned to support its customers and partners worldwide. Our team of over 50,000 employees, including 10,000+ R&D engineers, is dedicated to driving innovation and delivering high-quality, reliable solutions that meet the evolving needs of our customers.

At the core of ST's mission is a strong commitment to sustainability. As part of our vision for a greener future, ST has pledged to achieve carbon neutrality by 2027, embedding environmental and social responsibility into every aspect of our operations.

Through collaboration, innovation, and a relentless focus on excellence, STMicroelectronics continues to be a trusted partner for industries and organizations worldwide, enabling technologies that make a positive impact on people's lives and the planet.

Media sponsor: Yole Group is an international company recognized for its expertise in the analysis of markets, technological developments, and supply chains, as well as the strategies of leading players in the semiconductor, photonics, and electronics sectors.

With a relationship of trust established over the years, Yole Group maintains regular interactions with these leading companies, aiming to share and exchange its vision of markets and technologies.

Driven by committed and curious individuals, Yole Group benefits from this sharp expertise at the intersection of markets and technologies in the semiconductor industry, enabling it to offer a comprehensive and unique vision of the sector.

More information is available on the company's website: www.yolegroup.com.

Program at a glance

Monday September 15th

8:30am	Pre-Registration	
9:00am 1:00pm	**Short Course 1** Makalu ▶ Advanced Substrates for Chiplets, Heterogeneous Integration, and Co-Packaged Optics John Lau, Unimicron Technology Corporation	
2:00pm 6:00pm	**Short Course 3** Makalu ▶ From Wafer to Panel Level Packaging Tanja Braun, Fraunhofer IZM Markus Wöhrmann, Fraunhofer IZM	**Short Course 4** Kilimandjaro ▶ Electronic/Photonic Convergence Using Advanced Packaging: A Status Stéphane Bernabé, CEA LETI
5:00pm 6:00pm	**IEEE EPS Distinguished Lecture** Auditorium ▶ Recent Advances and Trends in Packaging John Lau, Unimicron Technology Corporation	

Tuesday September 16th

9:00am	Welcome & Conference Opening	
9:10am 9:55am	**Keynote 1** ▶ Propelling AI forward through Advanced Packaging Creativity	
9:55am 10:40am	**Keynote 2** ▶ The Interconnect 'Panelization'	
	Break – Exhibition	
11:15am 12:30pm	**Session 1A** Auditorium ▶ IC Packaging	**Session 1B** Kilimandjaro ▶ Interconnection Technologies
	Lunch – Exhibition	
1:50pm 3:05pm	**Session 2A** Auditorium ▶ Design, Modelling and Simulation	**Session 2B** Kilimandjaro ▶ Interconnection Technologies
	Break – Exhibition	
3:40pm 4:25pm	**Keynote 3** ▶ Mass Transfer: How the Push for MicroLED Displays Opens New Paths to Heterogeneous Integration	
	Room Change	
4:35pm 5:50pm	**Session 3A** Auditorium ▶ Materials	**Session 3B** Kilimandjaro ▶ Power Electronics
6:00pm 7:30pm	Dinner: Tasting of regional products & Exhibitors' time	

	8:30am
Short Course 2 Kilimandjaro ► **Microelectronics packaging basics in practice!** Valerie Volant, STMicroelectronics	9:00am 1:00pm
Short Course 5 Mont Blanc ► **Fundamentals and Advanced Packaging Applications of Substrates and Interposers** Ivan Ndip, Fraunhofer IZM Venky Sundaram, 3D System Scaling LLC Habib Hichri, Ajinomoto Fine-Techno USA Corporation	2:00pm 6:00pm
	5:00pm 6:00pm

	9:00am
Ingu Yin Chang, Executive Vice President, ASE Inc. Auditorium	9:10am 9:55am
Laurent Herard, Group VP – Head of Back End Manufacturing & Technology R&D, STMicroelectronics Auditorium	9:55am 10:40am

Session 1C Mont Blanc ► **Quality and Reliability**	**Session 1D** Makalu ► **Assembly and Manufacturing**	11:15am 12:30pm

Session 2C Mont Blanc ► **Special Topics**	**Session 2D** Makalu ► **Materials**	1:50pm 3:05pm

Dr. Chris Bower, CTO and co-founder, X Display Company (XDC)., Inc. Auditorium	3:40pm 4:25pm

Session 3C Mont Blanc ► **Quality and Reliability**	**Session 3D** Makalu ► **Assembly and Manufacturing**	4:35pm 5:50pm
		6:00pm 7:30pm

Program at a glance

Wednesday September 17th

9:00am 9:45am	**Keynote 4►** Recent Trends in Automotive Power Module Designs and Technology for Traction Inverters	
9:45am 10:30am	**Keynote 5►** System Technology Co-optimization for Advanced 3D & Heterogeneous Integration	
	Break – Posters – Exhibition	
11:15am 12:30pm	**Session 4A** ⚲ Auditorium ► Assembly and Manufacturing	**Session 4B** ⚲ Kilimandjaro ► Design, Modelling and Simulation
	Lunch Break – Posters – Exhibition	
1:50pm 3:30pm	**Session 5A** ⚲ Auditorium ► Substrate Technologies	**Session 5B** ⚲ Kilimandjaro ► Optoelectronics
	Break – Posters – Exhibition	
4:05pm 5:20pm	**Session 6A** ⚲ Auditorium ► System in Package	**Session 6B** ⚲ Kilimandjaro ► Quality and Reliability
5:30pm	Bus transfer: Busses leaving venue for conference dinner	
7:00pm 10:00pm	Conference Dinner	

Thursday September 18th

8:45am 9:30am	**Keynote 6►** Advanced Packaging – The Key Technology for Chiplet Integration	
	Room Change	
9:40am 10:55am	**Session 7A** ⚲ Auditorium ► Smart Manufacturing	**Session 7B** ⚲ Kilimandjaro ► IC Packaging
	Break – Exhibition	
11:30am 12:45pm	**Session 8A** ⚲ Auditorium ► Materials	**Session 8B** ⚲ Kilimandjaro ► Assembly and Manufacturing
	Lunch – Exhibition	
2:00pm 2:45pm	**Keynote 7►** Charting a Path for the Chiplet Era and Beyond	
2:45pm 3:15pm	**Awards and Closing**	⚲ Auditorium

Dr. Uwe Hansen, VP Power Component Development, Bosch Auditorium		9:00am 9:45am
Sébastien Dauvé, CEO, CEA-Leti Auditorium		9:45am 10:30am
Session 4C Mont Blanc ► **IC Packaging**	**Session 4D** Makalu ► **Poster Session #1**	11:15am 12:30pm
Session 5C Mont Blanc ► **Emerging Technologies**	**Session 5D** Makalu ► **Poster Session #2**	1:50pm 3:30pm
Session 6C Mont Blanc ► **Materials**		4:05pm 5:20pm
		5:30pm
		7:00pm 10:00pm

Prof. Dr.-Ing. Ulrike Ganesh, Managing Director, Fraunhofer IZM Auditorium		8:45am 9:30am
Session 7C Mont Blanc ► **Interconnection Technologies**	**Session 7D** Makalu ► **Inspection and Test**	9:40am 10:55am
Session 8C Mont Blanc ► **Power Electronics**		11:30am 12:45pm
Craig Bishop, Chief Technology Officer, Deca Technologies Auditorium		2:00pm 2:45pm
		2:45pm 3:15pm

Conference Area Map

What	Where	When
Opening, closing, keynotes	Auditorium	Tuesday Thursday
Oral presentations	Auditorium, Makalu Mont-Blanc, Kilimandjaro	Tuesday Thursday
Exhibition	Atrium	Tuesday Thursday
Coffee & Lunch breaks	Atrium	Tuesday Thursday

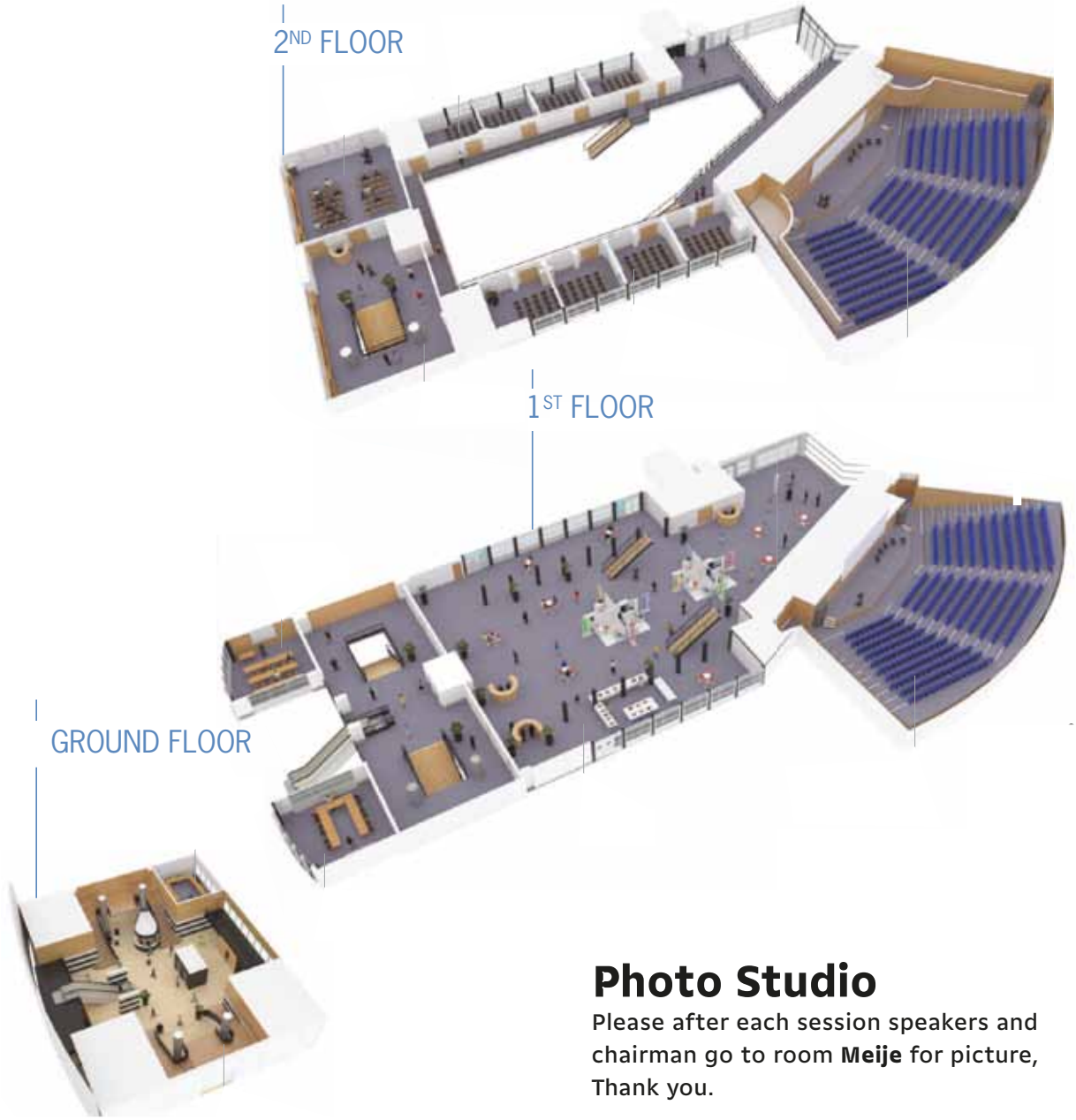

Photo Studio

Please after each session speakers and chairman go to room **Meije** for picture, Thank you.

Steering Committee

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Gabriel Kopp, VALEO, France
Tekfouy Lim, Fraunhofer IZM, Germany
Laurent Mendizabal, CEA – LETI, France
Jens Müller, TU Ilmenau, Germany
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Valérie Volant, STM, France
Nadia Wazad, AIRBUS DEFENCE AND SPACE, France
Chunyan Yin, Southeast University, China
Sung-Uk Zhang, Dong-Eui University, South Korea
Christophe Zinck, ASE Group, France
Zdravko Zojceski, VALEO, France

Professional Development Courses

Short Course 1

Advanced Substrates for Chiplets, Heterogeneous Integration, and Co-Packaged Optics

John Lau
Unimicron Technology Corporation

John Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging, has published more than 535 peer-reviewed papers (385 are the principal investigator), 52 issued and pending US patents (31 are the principal inventor), and 24 textbooks (all are the first author). John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.

▷ Abstract

Today, most of the package substrates for HPC driven by AI (artificial intelligence) are made by the 2.5D IC integration. In general, for 2.5D or CoWoS (chip on wafer on substrate), the SoC and high bandwidth memories (HBMs) are supported by a TSV-interposer and then solder bump and underfill on a build-up package substrate. However, because of the ever-increasing size of the TSV-interposer, the manufacturing yield loss of the TSV-interposer is becoming unbearable. The key players such as NVIDIA, AMD, Intel, SK Hynix, Samsung, Micron, TSMC, etc. are working very hard to eliminate the TSV interposer and put the HBMs directly on top of the SoC (3.3D IC integration). Front-end integration of some of the chiplets (before package heterogeneous integration) can yield a smaller package size and a better performance (3.5D IC integration). In the past few years, 2.3D IC integration or CoWoS-R is getting lots of traction. The motivation is to replace the TSV-interposer with a fan-out fine metal L/S redistribution-layer (RDL)-substrate (or organic-interposer). In general, for 2.3D, the package substrate structure (hybrid substrate) consists of a build-up package substrate, solder joints with underfill, and the organic-interposer. Today, 2.3D is already in production. Recently, TSMC published two papers on replacing the large-size TSV-interposer by LSIs (local silicon interconnects, i.e. Si bridges) and embedding the LSIs in fan-out RDL-substrate. TSMC called it CoWoS-L. Recently, since Intel's announcement on the glass core substrate for their one-trillion transistors to be shipped before 2030, glass core substrate has been a very hot topic. Since the shipments of co-packaged optics (CPO) by Intel and Broadcom CPO have been getting lots of traction. In this lecture, the introduction, recent advances, and trends in the substrates of 3.5D IC integration, 3.3D IC integration, 3D IC integration, 2.5D IC integration, 2.3D IC integration, 2.1D IC integration, 2D IC integration, fan-out RDL, embedded Si-bridge, CoWoS-R, CoWoS-L, CPO, and glass core for HPC driven by AI will be discussed. Some recommendations will be provided.

Short Course 2

Microelectronics packaging basics in practice!

Valerie Volant
STMicroelectronics

After studying Materials Science at Polytech Grenoble, I reached microelectronics packaging world 25 years ago. I have worked for several companies such as Teledyne E2V and Tronics Microsystems, performing various missions from R&D to industrialization and production support. Still in the packaging field, I joined STMicrolectronics Operations 4 years ago to introduce new products on assembly lines and support innovation projects. My knowledge of microelectronics packaging technology has enabled me to join STM's expert staff. In parallel, I'm involved in Imaps France, a packaging association, and Polytech Grenoble School. I am also engaged in educational volunteering to promote high technologies, particularly microelectronic packaging and its values.

▷ Abstract

This course has a seminar-like approach, it is NOT aimed at people who already consider themselves as packaging experts.

The course is suitable for:

- students, in material science or IC design, electronics, or microelectronics
- people collaborating with packaging engineers: such as marketing, sales, components test, IC design, application development, or device characterization. So, everyone not so close to packaging technologies, but curious about them…

After a theorical presentation on the basics of packaging, covering the main steps, machines, physical and industrial critical points, you will have to apply these newly learnt notions in practice, by identifying suitable packaging solutions to meet a specific product requirement…

The purpose of this handmade packaging experiment is to gain a better understanding of the challenges faced by packaging engineers in their daily work, and to realize the fundamental role of microelectronics packaging in enabling an IC die to become the expected product.

Note : the practical exercise limits the course to 12 attendees

Short Course 3

From Wafer to Panel Level Packaging

Tanja Braun
Fraunhofer IZM

Tanja Braun studied mechanical engineering at Technical University of Berlin and joined Fraunhofer IZM in 1999. In 2013 she received her Dr. degree for the work focusing on humidity diffusion through particle-filled epoxy resins. Tanja Braun is head of the department System Integration and Interconnection Technologies. Recent research is focused on fan-out wafer and panel level packaging and technologies Tanja Braun was leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin.

Markus Wöhrmann
Fraunhofer IZM

Markus Wöhrmann received the M.Sc. in electrical engineering at Technical University of Berlin in 2010. Since 2010 he is working on electrical and mechanical property estimation of thin film layers at the Technical University of Berlin. In 2016 he joined the Fraunhofer IZM. He is leading the group "Lithography and Thin Film Polymers for Wafer-Level-Packaging" at the Fraunhofer IZM since 2019, where he is responsible for process development of RDL processing for Fan-In and Fan-out Wafer Level Packaging.

▷ Abstract

Wafer and Panel Level Packaging are two of the dominating trends in microelectronics packaging. Both approaches with different flavors as RDL last face-up or face-down have reached maturity and are introduced in high volume manufacturing. Main driver for moving from wafer to panel level packaging is of course lowering the packaging cost. More packages can be processed in parallel and panel formats have a much better area utilization (ratio between panel/wafer size and package size) than round wafer shapes. With the advent of chiplet technology and the application to large body size packages e.g. HPC modules Panel Level Packaging is actually gaining momentum as an option for lower cost and high-density packaging. The PDC will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging. This will include material and process discussion, technologies, equipment, applications and market trends as well as cost and environmental aspects.

The PDC will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging. This will include material and process discussion, technologies, equipment, applications and market trends as well as cost and environmental aspects.

Outline

1. Introduction to Advanced Packaging
2. Trends in Wafer Level Packaging
3. Fan-In and Fan-out on Wafer Level: Material, Processes, Applications
4. Introduction and Definition Panel Level Packaging
5. Fan-out Panel Level Packaging: Technologies, Challenges and Opportunities
6. Cost & Environment Modelling

Who Should Attend

Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer Level Packaging and the transition to Panel Level Packaging. Engineers and manages are welcome as detailed technology descriptions as well as market trends, applications and cost modelling are presented.

Short Course 4

Electronic/Photonic Convergence Using Advanced Packaging: A Status

Stéphane Bernabé
CEA LETI

Stéphane Bernabé (Member, IEEE) received the M.Sc. degree in Physics and Photonics engineering from the University Louis Pasteur of Strasbourg, France, in 1997, and Ecole Nationale Supérieure de Physique de Strasbourg (ENSPS). In 2007 he joined CEA-LETI , Optics and Photonics Department, and has been involved in several research dealing with optoelectronic device packaging and application of Silicon Photonics to Data communications and optical Networks on Chips (oNoC) for computing. He is now heading the Photonics Packaging Lab at CEA-LETI. He has published 60 papers, 17 patents, and co-authored 3 book chapters. His current interests are in Photonic/Electronic co-integration, and PIC optical coupling. He is an IEEE EPS member and ECTC technical committee.

▷ Abstract

The recent development of silicon photonics and the opportunities it represents for addressing a number of challenges in the fields of HPC/AI, datacom and sensors have accelerated the convergence of electronic and photonic components. This combination of both technologies cannot be achieved without recourse to advanced packaging. Here, we review the challenges and technologies enabling this paradigm shift, focusing on the underlying physics and the expected developments.

This short course will deal with the following topics:

- Silicon Photonics: basics on devices , modules and applications
- Evolving needs in data transmission, Ethernet switches roadmap
- A short story of early Electronic/ Photonics integration
- Co-packaging optics : the challenges
- 3D packaging building blocks
- The coupling challenge
- Recent demonstrations of CPO integration
- Outlook, photonics interposers

Short Course 5

Fundamentals and Advanced Packaging Applications of Substrates and Interposers

Ivan Ndip
Fraunhofer IZM

Venky Sundaram
3D System Scaling LLC

Habib Hichri
Ajinomoto Fine-Techno USA Corporation

▷ Abstract

Substrate and interposer technologies play a significant role in the cost, performance and reliability of electronic packages, components and systems. In this PDC, the fundamentals, and advanced packaging applications of organic, ceramic, silicon and glass substrate technologies as well as interposers will be presented and extensively discussed.

The PDC is structured into two three main sections, namely, a) applications driving advanced packaging and heterogeneous integration, b) advanced substrates technologies and c) interposer technologies.

In the first section, emerging applications that drive innovations in advanced packaging substrates and interposer technologies will be presented. This includes applications in the fields of wireless communication, radar sensing, high performance computing (HPC) and AI in a wide range of industries.

The second section will commence with an in-depth examination of advanced substrate technologies, materials and processes, including high-density organic laminates, glass and silicon substrates. Recent breakthroughs in substrate fabrication processes, including advanced lithography, laser drilling, and metallization techniques will be highlighted. Attendees will gain practical insights into overcoming common challenges like warpage control, fine-pitch routing, and multilayer RDL, ensuring reliability and manufacturability in next-generation electronic packages. Furthermore, methods for measuring the relative dielectric constant (Dk) and loss tangent (Df) of substrate materials from 1 GHz to over 100 GHz will be presented and demonstrated for a wide range of substrates, including organic laminates, thin-film RDL polymers, mold, glass, silicon and Ajinomoto Build-Up Films (ABF).

Recent developments in silicon, glass and organic-based interposer technologies will be presented in the last section of the PDC. The application of interposers for the development of chiplets, especially for HPC and AI applications, will be extensively discussed. Die-to-die (D2D) interconnects for chiplets, and UCIe (Universal Chiplet Interconnect Express) specifications will also presented. Participants will learn more about the integration of 2.5D and 3D packaging solutions, and the role of interposers in enabling heterogeneous integration. The pros and cons of silicon, glass and organic interposers will also be discussed.

Finally, guidelines for selecting substrate and interposer technologies as well as materials and processes for application-specific advanced packaging and heterogeneous integration will be given.

Outline

1. Applications driving innovations in advanced packaging and heterogeneous integration
2. Fundamentals of advanced substrate technologies, materials and processes, including high-density organic laminates, glass and silicon substrates
3. Measured Dk and Df values of substrate materials from 1 GHz to over 100 GHz
4. Fundamentals of silicon, glass and organic-based interposer technologies
5. Pros and cons of silicon, glass and organic interposers
6. Chiplets, die-to-die (D2D) interconnects and UCIe
7. Guidelines for selecting substrate and interposer technologies for application-specific advanced packaging and heterogeneous integration

Keynotes EMPC 2025

Keynote 1

Propelling AI forward through Advanced Packaging Creativity

Ingu Yin Chang

Executive Vice President, ASE Inc.

Ingu Yin Chang is the Executive Vice President at ASE Inc., based in Sunnyvale, California. In his current role, he is responsible for developing and executing sales strategy, while driving global initiatives for ASE's expanding packaging, systems, and integration solutions portfolio. Prior to joining ASE in 2013, Yin was CEO of Vertical Circuits Inc. (VCI), a company focused on the development of next generation vertical interconnect for next generation silicon integration. Previously, Yin performed a variety of management roles covering sales and operations at Amkor with responsibility for the Greater China region. He has over thirty years of leadership experience in executive management, sales, business development, IP management and strategic alliances. Yin received his material science engineering degree from University of California, Berkeley.

▷ Abstract

The semiconductor industry is stacked with groundbreaking innovation that is helping to weave intelligence into every dimension of life, through generative, agentic and physical AI models, spanning all the way from the cloud to the edge. Heterogeneous Integration through advanced packaging is playing a pivotal role in pushing physical, electrical, and thermal limits to achieve better energy efficiency and greater compute power. During his keynote, ASE's Yin Chang will set the stage by exploring the AI landscape, highlighting challenges that require our collective attention, particularly as we move from electrons to photons. He will then expand on how advanced packaging creativity is propelling AI forward by integrating higher-performance chips within smaller form factors for transformative latency improvement and bandwidth enhancement.

Keynote 2

The Interconnect "Panelization"

Laurent Herard

Group VP – Head of Back End Manufacturing & Technology R&D, STMicroelectronics

Laurent Heard received an Engineering Degree in physics of semiconductor from the INP Grenoble France. He has thirty-two years of experience in Packaging technology R&D and Back End assembly manufacturing in Europe, Morocco, Singapore and Malaysia. Laurent is a Company Fellow in the field of packaging and interconnect technology

▷ Abstract

The very fast innovation pace on AI processing hardware is pushing the semiconductor packaging industry to set up high volume production capability for ultra large very high-density interconnection interposers. This is creating a strong momentum for high density fan out Panel Level Packaging (PLP).

In the domain of electrification, there is a race to power density and efficiency. This is fueling the industry for designing and industrialize new ways to interconnect power chips with drivers and passives for low electrical losses, typically low RdsOn and low stray inductance.

Those two domains have very different requirements in terms of interconnect density and current capability, but they share the same technology trend with the integration of latest innovations from different interconnection manufacturing concepts: PCB, high density substrate, wafer level packaging, embedded die and passives, and traditional packaging technology such copper pillar flip chip, die attach sintering.
This presentation gives an overview of the Panel Level Packaging technology trends for main semiconductor applications. Then it presents the experience and key challenges faced during the industrialization of an actual high volume PLP manufacturing line.

Keynote 3

Mass Transfer: How the Push for MicroLED Displays Opens New Paths to Heterogeneous Integration

Dr. Chris Bower
CTO and co-founder, X Display Company (XDC)., Inc.

Chris Bower is the Chief Technology Officer and co-founder of X Display Company (XDC). Before joining XDC, he was the Chief Technology Officer at X-Celeprint Limited, a company founded to develop and commercialize advanced micro assembly technologies. He was formerly a Technical Manager at Semprius, Inc., where he led the team responsible for elastomer-stamp mass transfer of silicon integrated circuits and compound semiconductor solar cells. His research interests include three-dimensional integration of integrated circuits, heterogeneous integration of compound semiconductors onto non-native substrates and the fabrication of low-cost, large-format electronics using novel assembly methods. He has co-authored over one hundred and thirty scientific publications and over one hundred and fifty patent applications.

▷ Abstract

Assembling microLEDs into displays is challenging due to the need for precise placement of millions of tiny microLEDs. Fluidic self-assembly, laser transfer, and stamp transfer are all candidate technologies. Among these, elastomer stamp transfer has proven to be a scalable, high-yield solution. The advancements in mass transfer technology are now being applied to heterogeneous integration challenges beyond displays, enabling improved performance and flexibility in combining different types of components into complex electronic systems.

Keynote 4

Recent Trends in Automotive Power Module Designs and Technology for Traction Inverters

Dr. Uwe Hansen

VP Power Component Development, Bosch

Uwe Hansen received his PhD in Physics at the Technical University from Munich.

He specialized in theoretical semiconductor physics. Uwe started his career at Bosch as a process engineer in the Bosch automotive Wafer fab, held various functions within Bosch related to semiconductors and was responsible for advanced packaging for CE and automotive MEMS. Since 2018 he is heading the department for power component and module development at Bosch.

▷ Abstract

In order to reduce the clearly visible trend of global warming, the changeover from fossil fuels to electrification is driven forward. Since transport largely contributes to C02 emissions the electrification of Plug-in Hybrid Electric Vehicles and Electric Vehicles is crucial. In this dynamic field power modules are needed that find the right balance between conflicting requirements like power density, scalability, design flexibility and performance. The challenge with modules in comparison to discrete is that part of the circuity is included in the module and that no standard is defined. In addition, due to the very different material and physical properties of wide band gap materials like SiC, learnings from the Si world can only be used to a limited extend. Emerging from the two different trends – frame-based modules and molded modules – a concept combining the best of both and enabling 3D routing will be presented. The talk concludes with an outlook towards standardization due to the request for 2nd source capability.

Keynote 5

System Technology Co-optimization for Advanced 3D & Heterogeneous Integration

Sébastien Dauvé

CEO, CEA-Leti

Sébastien Dauvé was named CEO of CEA-Leti effective on July 1, 2021, after more than twenty years of experience in microelectronics technologies and their applications, including clean mobility, medicine of the future, cybersecurity, and power electronics.

Sébastien Dauvé started his career at the French Armament Electronics Center, where he worked on developing synthetic-aperture radar. In 2003, he joined CEA-Leti as an industrial transfer manager and supervised several joint research laboratories, in particular with the multinational Michelin.

In 2007, Sébastien Dauvé became a laboratory manager, then head of an R&D department in the area of sensors applied to the Internet of things and electric mobility. During this time, he supported the dissemination of new technologies in industry, including the automotive industry (Renault), aeronautics, national defense (SAFRAN), and microchips with the industry leader Intel. He played an active role in the creation of start-ups in application fields ranging from health to infrastructure security, leading to dozens of new jobs. In 2016, he became Director of the CEA-Leti Systems Division.

From sensors to wireless communication, Sébastien Dauvé has played an active role in the digital transformation, focused on coupling energy frugality and performance. He has made cross-disciplinary approaches central to innovation by harnessing the expertise of talented teams with diverse backgrounds. Their goal is to provide technological tools for meeting the major societal challenges of the future.

Sébastien Dauvé is a graduate of the French Ecole Polytechnique and the National Higher French Institute of Aeronautics and Space (ISAE-SUPAERO).

▷ Abstract

The world's digitalization is driving an enormous increase in data generation, expected to reach nearly 500 zettabytes by 2030. This data deluge leads to a dramatic rise in energy consumption, which is unsustainable in the medium term. Technological breakthroughs must be developed to significantly improve (by a factor of 1000) the power efficiency of electronics. Today, it is clear that a single technology cannot meet all the requirements of the most demanding computing and connectivity ICs. It is thus evident that heterogeneous 3D integration or advanced packaging is the way forward to combine different technologies and also enable novel architectures (such as chiplets) that bring various functions closer together. This talk will detail the different technologies under development, such as hybrid bonding, TSV (Through-Silicon Vias), interposers, and wafer-to-wafer or die-to-wafer approaches. Recent results and demonstrators will also be presented.

Keynote 6

Advanced Packaging The Key Technology for Chiplet Integration

Prof. Dr.-Ing. Ulrike Ganesh

Managing Director, Fraunhofer IZM

Professor Ulrike Ganesh has over 21 years of experience in the semiconductor industry. She is Managing Director of Fraunhofer IZM (Institute for Reliability and Micro integration) and a professor at the Technical University of Berlin, where she holds the Chair of "Design and Hetero-Integration of Micro-Electronic Systems." Throughout her career, she has worked with top companies including IBM, Qualcomm, and Bosch and research institutions in both Germany and the USA. Professor Ganesh earned her doctorate in electrical engineering from the Technical University of Berlin, specializing in failure analysis for semiconductor devices. Since her postdoctoral research, she has built and led teams focused on driving innovation. As head of Fraunhofer IZM, she is responsible for 450 experts in advanced semiconductor packaging. A passionate mentor, she actively supports the growth of young scientists and engineers. With her expertise in leadership, R&D, and strategic vision, she continues to shape the future of microelectronics.

▷ Abstract

Chiplets are becoming key components: They not only help tackle the forces that are threatening to end Moore's Law, they are also the crucial gateway technology for e.g. electro-optical systems, non-CMOS devices, and sensors, and they promise to sustain the race for high performance at low cost. Advanced packaging is key to the widespread acceptance of chiplets. With 30 years of experience in this field, Fraunhofer IZM plays a crucial role in the microelectronics community. The presentation will discuss the basics of chiplet integration and highlight their advantages over traditional monolithic

chips. It addresses the challenges in terms of reliability and the associated design and development requirements and highlights the need to consider design optimization, material selection, test procedures, fault tolerance, and continuous improvement holistically and from the beginning. A combination of these is essential to make chiplet systems meaningfully more reliable.

Keynote 7

Charting a Path for the Chiplet Era and Beyond

Craig Bishop

Chief Technology Officer, Deca Technologies

Craig Bishop is Chief Technology Officer at Deca Technologies, managing the Adaptive Patterning technology, EDA development, intellectual property, and R&D. He is also Technical Director for the $100M SHIELD USA program in close collaboration with ASU to produce leap-ahead organic substrates under the National Advanced Packaging Manufacturing Program (NAPMP). Prior, Craig was the architect of Adaptive Patterning at Deca where he developed the technology and design methodologies that have been implemented in high-volume production, with over seven billion devices shipped in leading smartphones and other electronics. Craig Bishop received his B.S. degree in electrical and computer engineering from the University of Arizona in Tucson with specialization in analog IC design. He has over than two dozen patents issued related to fan-out and electronic interconnects.

▷ Abstract

The chiplet era is upon our industry, driving exponentially increasing demand for die-to-die interconnect that is met with an expanding variety of package architectures. Interposers, hybrid bonding, and novel substrate technologies are approaching the scale of upper metals layers in a chip, driven by insatiable demand from artificial intelligence and high-performance computing applications. As electronic design automation tools catch up to these advancements, designers will completely blur the boundary between chip wires and package wires. Beyond these widely discussed applications, chiplets are coming for microcontrollers too, enabling the disaggregation of non-volatile memory, analog, and digital blocks. This talk will explore macro trends of the chiplet era and contemplate what path lies beyond – perhaps the monolithic decades will become a brief historical exception.

Posters session
Session #1

Thermomechanical Study for Stress-management of Silicon Photonics Interposers
Céline Feautrier, Benoit Saudet, Jean Charbonnier, Edouard Deschaseaux, Damien Saint-Patrice, Rémi Vélard, Myriam Assous
Université Grenoble Alpes, CEA, Leti, Grenoble, France

Reusing SMD Components on E-textiles: An Ageing Study by Combination of Corrosive Gases and Washing
Martin Hirman, Jiri Navratil, Andrea Benesova, Frantisek Steiner
University of West Bohemia, Faculty of Electrical Engineering, Czech Republic

A Comparative Study of Silver Sintering Pastes for Die-attach Applications: Microstructure, Mechanical Properties, and Reliability
Jiri Hlina[1], Martin Hirman[1], David Michal[1], Pavel Rous[1], Martin Janda[1], Filip Kulhanek[2]
1. University of West Bohemia, Pilsen, Czech Republic
2. Elceram a.s., Hradec Kralove, Czech Republic

Design and Evaluation of a Perforated Dielectric Flat Lens Antenna Array for D-band Applications
Yen Ting Wang, Po-An Lin, Huei-Shyong Cho, Shih-wen Lu, Wei-Tung Chang
Advanced Semiconductor Engineering, Inc., Taiwan

A High Gain Antenna-in-Package (AiP) with Horn Structure for D-band Applications
Po-An Lin, Shao-En Hsu, Shih-Wen Lu, Yu-Chang Chen, Jen-Chieh Kao
Advanced Semiconductor Engineering, Inc. (ASE), Taiwan

Fine-pitch Flip-chip Bonding Process with Laser Non-conductive Paste (NCP) and Laser-assisted Bonding (LAB) for High-reliability
Ki-Seok Jang, Yong-Sung Eom, Gwang-Mun Choi, Jiho Joo, Jungho Shin, Jin-Hyuk Oh, Chan-Mi Lee, Ga-Eun Lee, Seong-Cheol Kim, Kwang-Seong Choi
ETRI, Korea, Republic of (South Korea)

Indium as the Superconducting Interconnect for Quantum Chiplets
Jowesh Avisheik Goundar[1], Mai Thi Ngoc La[2], Yugi Otake[2], Hideo Kosaka[1], Fumihiro Inoue[3]
1. Institute of Advanced Sciences, Yokohama National University, Japan
2. Graduate School of Engineering, Yokohama National University, Japan
3. Faculty of Engineering, Yokohama National University, Japan

Test Equipment for Sensor Interfaces Emulated by Generic Electronic Control Unit
Nicolae Ioan Gross, Paul Svasta
National University of Sciences and Technologies Politehnica, Bucharest, Romania

Grain Orientation Analysis for Thermal Cycling Evaluation of Die-attach Solder Joints
Hiroaki Tatsumi[1], Yujiro Hayashi[2,3], Jaemyung Kim[2], Makina Yabashi[2,3], Hiroshi Nishikawa[1]
1. The University of Osaka, Japan
2. RIKEN SPring-8 Center, Japan
3. Japan Synchrotron Radiation Research Institute, Japan

Thermal Fatigue Resistance Improvement of New Al Bonding Wire
Motoki Eto[1], Noritoshi Araki[1], Tomohiro Uno[3], Sandy Klengel[2], Robert Klengel[2], Daizo Oda[1]
1. Nippon Micrometal Corporation, Japan
2. Fraunhofer-Institute for Microstructure of Materials and Systems IMWS
3. Nippon Steel Corporation

Thermal Analysis of Power Electronic Modules with Parametric Model Order Reduction
Sheikh Hassan[1], Mark Sherriff[2], Pearl Agyakwa[2], Paul Evans[2], Stoyan Stoyanov[1]
1. School of Computing and Mathematical Sciences, University of Greenwich, London, United Kingdom
2. Department of Electrical and Electronic Engineering, University of Nottingham, Nottingham, United Kingdom

Photoresist/Polymer Removal Optimized Chemistry with Adding Hydrogen Radical in MEMS Process Fabrication and Other Applications with HDRF®
Marc Segers, Giovanni Terenziani, Safia Benkoula
Plasma-Therm Europe, France

Session #2

Flip-chip Bonded Hybrid Germanium X-ray Detectors Suitable for Operating with Thermal Gradient Between Sensor and ASIC

Andreas Schneider[1], James Hollingham[1], Alexander Dainty[1], Toby G. Brookes[1], John David Lipp[1], Matthew David Wilson[1], Marcus Julian French[1], Marcello Borri[2], Konrad Sutowski[2], Daniel Thacker[2], Matthew Buckland[2], Andrew Hill[2], William Helsby[2]
1. STFC-RAL, United Kingdom
2. STFC-DL, United Kingdom

Thermal Management of an Electronic Module Made by a Solderless Assembly Method

Gaudentiu Varzaru[1], Roxana Tulea[1], Madalin Moise[2], Mihai Branzei[3], Paul Svasta[2]
1. Syswin Solutions, Romania
2. Electronic Technology & Reliability Department, National University of Science and Technology Politehnica Bucharest, Romania
3. Department of Metallic Materials Sciences, Physical Metallurgy, Faculty of Materials Science and Engineering, National University of Science and Technology Politehnica Bucharest, Romania

Selective Micro Laser Melting: Influence of Scan Speed and Laser Power on Interconnect Morphology and Performance

Arun Kumar Sivakumar, Manish Arora
Indian Institute of Science, Bengaluru, India

Flip Chip Bonding of PMUT Using Adhesives and their Effect on Electrical Performance

Muhammad Hassan Malik, Zhou Da, Rodrigo Tumolin Rocha, Chunlei Xu
Silicon Austria Labs

Automated Non-destructive Mechanical Testing of Fine Pitch Wirebond Arrays

Lyle Alexander Menk
Sandia National Laboratories, United States of America

Power Modules: Crack and Shrinkage Phenomenon

Adeline Liger, Vincent Charlot, Jean-Christophe Leroux
Protavic, France

Void Inspection Using Stress Field Imaging in Densely Patterned Bonded Wafers

Zsolt Kovács[1], Csenge Dobos[1], Gábor Molnár[1], Zsolt Kovács[1], György Nádudvari[1], Zoltán Kiss[1], Delphine Le Cunff[2], Maximilien Dallery[1]
1. Semilab Co. Ltd., Hungary
2. STMicroelectronics SA

Temperature Profile Optimization for Vacuum Soldering of Components on Heat Sink

František Steiner[1], Martin Hirman[1], Pavel Rous[1], Václav Wirth[2]
1. University of West Bohemia, Czech Republic
2. Rohde & Schwarz závod Vimperk, s.r.o., Czech Republic

Investigating the Dynamic Bending Behaviour of Biodegradable Printed Circuit Boards

Oliver Krammer, Patrik Kovács, Attila Géczy
Budapest University of Technology and Economics, Hungary

Stacked and Staggered Vias in FR4 Laminate for Special Application

Aneta Cholaj, Krzysztof Lipiec, Andrzej Kiernich, Dariusz Ostaszewski, Miroslaw Kozlowski, Marek Koscielski, Adam Lipiec, Janusz Borecki
Łukasiewicz Research Network - ITR, Poland

Engineering Dual Alloy Solder Paste Systems to Achieve High Reliability, Energy Savings, Withstand High Junction Temperatures

Karthik Vijay, Graham Wilson
Indium Corporation, United Kingdom

Warpage Reduction of Laminate Substrates Through Metamodel-based Optimization of Material Properties

Fredy John Porathur[1,2], Fabian Huber[1], Eduard Stadler[1], Peter Filipp Fuchs[3], Dieter Paul Gruber[2,4]
1. CSA R&D ET Packaging Development, Materials and Simulation- ams OSRAM AG, Premstaetten, Austria
2. Institute of Materials Science and Testing of Polymers- Montanuniversität Leoben, Leoben, Austria
3. Simulation and Modeling- Polymer Competence Centre Leoben (PCCL) GmbH, Leoben, Austria
4. Surface Testing, Robot Vision and Artificial Intelligence- Polymer Competence Centre Leoben (PCCL) GmbH, Leoben, Austria

Innovative Deposition Solution for TSV Integration and Conformal Deposition of Oxide, Nitride, and Metal Layer with Dual Frequency Pulsed Equipment, Application of Low Temperature Deposition of Dielectric Layer

Marc Segers, Pierre-David Szkutnik, Safia Benkoula
Plasma-Therm Europe, France

Conference Agenda

Monday September 15th

8:30am 6:00am	Pre-Registration	
9:00am 1:00pm	**Short Course 1** — Makalu ► **Advanced Substrates for Chiplets, Heterogeneous Integration, and Co-Packaged Optics** John Lau, Unimicron Technology Corporation	
2:00pm 6:00pm	**Short Course 3** — Makalu ► **From Wafer to Panel Level Packaging** Tanja Braun, Fraunhofer IZM Markus Wöhrmann, Fraunhofer IZM	**Short Course 4** — Kilimandjaro ► **Electronic/Photonic Convergence Using Advanced Packaging: A Status** Stéphane Bernabé, CEA LETI
5:00pm 6:00pm	**IEEE EPS Distinguished Lecture** — Auditorium ► **Recent Advances and Trends in Packaging** John Lau, Unimicron Technology Corporation	

Tuesday September 16th

9:00am	Welcome & Conference Opening
9:10am 9:55am	**Keynote 1** ► Propelling AI forward through Advanced Packaging Creativity
9:55am 10:40am	**Keynote 2** ► The Interconnect 'Panelization'

Break – Exhibition

11:15am	**Session 1A** — Auditorium **► IC Packaging** **Development of Die Attach Process for Thin Device Using a Novel High Thermal Conductivity Pressure-less Semi-sintering Paste with Capillary Filling Technology** Shogo Nakano, Sumitomo Bakelite Co., Ltd. Nicoletta Modarelli, STMicroelectronics **A Novel Package Technology for Better MOSFET Performance** Ilyas Dchar, Nexperia **Fan Out Wafer Level Packaging – Towards a European Manufacturing Supply Chain** Marc Dreissigacker, AEMtec GmbH	**Session 1B** — Kilimandjaro **► Interconnection Technologies** **Material Strategy and Challenges for Fine Interconnection in Advanced Packages** Kazuyuki Mitsukura, Resonac **Stability of the Superconducting β-Sn Phase at Low Temperatures for 3D Cryogenic Packaging** Meriem Guergour, CEA-Leti **Integration of Photo-imaging Technology and Microvias in LTCC for Enhanced High-frequency Applications and Packaging** Birgit Manhica, Fraunhofer IKTS
12:30pm		

		8:30am 6:00am
Short Course 2 Kilimandjaro ▶ **Microelectronics packaging basics in practice!** Valerie Volant, STMicroelectronics		9:00am 1:00pm
Short Course 5 Mont Blanc ▶ **Fundamentals and Advanced Packaging Applications of Substrates and Interposers** Ivan Ndip, Fraunhofer IZM Venky Sundaram, 3D System Scaling LLC Habib Hichri, Ajinomoto Fine-Techno USA Corporation		2:00pm 6:00pm
		5:00pm 6:00pm

	9:00am
Ingu Yin Chang, Executive Vice President, ASE Inc. Auditorium	9:10am 9:55am
Laurent Herard, Group VP – Head of Back End Manufacturing & Technology R&D, STMicroelectronics Auditorium	9:55am 10:40am

Session 1C	Session 1D	
Session 1C Mont Blanc ▶ **Quality and Reliability**	**Session 1D** Makalu ▶ **Assembly and Manufacturing**	**11:15am**
Defining a Scalable Test Methodology to Deliver High Quality AI Products Soumya Padmanabha, Meta Platforms Inc.	**Development of Advanced Screen-printing Technology for Flip-chip Transfer of Electronic Components** David Henry, CEA	
Embedding of components as an effective way to achieve high reliability for special applications products Marek Koscielski, Łukasiewicz Research Network - ITR	**Thinning and Dicing Process Integration of High Accuracy Using A Novel Self-assembly Stage for Chip on Wafer** Tadatomo Yamada, Lintec Corp.	
Assessment of QFN Assemblies' Thermal Strain Characterization and its Evolution Through Thermal Cycling Aging Vincent Sisomseun, MBDA France	**A Study of 355 nm UV Laser Ablation Process for Singulation of Silicon Wafers** Serguei Stoukatch, Microsys lab	**12:30pm**

Lunch – Exhibition

1:50pm – 3:05pm

Session 2A — Auditorium
► Design, Modelling and Simulation

A Methodology for Modeling Capillary Underfill (CUF) in Advanced Packaging
Dariush Ghaffari Tari, Henkel

Simulation-based Analysis of Thermal Effects Induced by RF Interference in MEMS Microphones
Yogesh Babu, Rosenheim University of Applied Sciences

Numerical Case Study of Stress and Plastic Strain Distributions in BGA Solder Balls by Comparison of a Novel Inorganic Encapsulation and Conventional Underfill Variants
Alexander Reichel, Fraunhofer Institute for Microstructure of Materials and Systems

Session 2B — Kilimandjaro
► Interconnection Technologies

Characterization of Chip-to-wafer Interconnects with Thick Gold Finish for Fan-out Wafer-level Packaging RDL First Integration
Arnaud Garnier, CEA-Leti

Fine-pitch Die-to-wafer Bonding Technologies for Chiplet Integration
Juliana Panchenko, Fraunhofer IZM

Fabrication of Indium Interconnections for Flip-chip Assembly on Single Die
Mel Dehays, CEA

Break – Exhibition

3:40pm – 4:25pm **Keynote 3** ► Mass Transfer: How the Push for MicroLED Displays Opens New Paths to Heterogeneous Integration

Room Change

4:35pm – 5:50pm

Session 3A — Auditorium
► Materials

Exploration of Cu Interfacial Engineering to Enhance Cu Interconnects Reliability
Oliver Chyan, University of North Texas

Tailored Polymers for Wafer-level Optics Manufacturing via Nanoimprint Lithography
Patrick Schirmer, DELO Industrial Adhesives

Evaluations of Transient Liquid Phase Joints Using In-coated Ag Sheet
Hiroshi Nishikawa, University of Osaka

Session 3B — Kilimandjaro
► Power Electronics

Promoting EMC Adhesion to Copper Leadframe Through Oxide Thickness Optimization
Céline Feautrier, CEA-Leti

Thermal and Structural Analysis of GaN Layers on Foreign Substrates for Vertical Power Devices
Verena Leitgeb, Materials Center Leoben Forschung GmbH

The next generation die top system (Ag-only DTS®) for Cu wire bonding on SiC chips
Thorsten Vehoff, Heraeus Electronics

6:00pm – 7:30pm Dinner: Tasting of regional products & Exhibitors' time

Session 2C Mont Blanc ► Special Topics **Advanced Dielectric Films for Fusion Bonded 3D Integration** Taisuke Yamamoto, Yokohama National University **A Miniaturized Dual Band (28/39 GHz) AiP Design for Millimeter-Wave 5G Mobile Phone Applications** Yen Ting Wang, ASE group **Development of a 3D Quilt Packaging Method for Implantable Applications** Chloé Bernardoni, Imperial College London	**Session 2D** Makalu ► Materials **Bi–in Segregation in Low-temperature SLID Bonding: Au-in-bi System** Gayathry Thampi, University of South Eastern Norway **Large Area (> 2500 mm²) Sintering at Sub 220°C with Micro-scale Copper Flakes** Olaf Rämer, Technische Universität Berlin **Influence of Total Encapsulation of White-light Mid-power LED Packages Over the Correlated Colour Temperature** Edward André Olivera Apaza, THD Technologie Campus Cham	1:50pm 3:05pm
Dr. Chris Bower, CTO and co-founder, X Display Company (XDC)., Inc. Auditorium		3:40pm 4:25pm
Session 3C Mont Blanc ► Quality and Reliability **Microstructural Characterization for the Joining Interface of Ag@Si Composite Sinter Joining for SiC Power Device by Scanning Transmission Electron Microscopy** Masahiko Nishijima, F3D system Integration Lab **Experimental and Numerical Investigation of the Impact of Surface Roughness of Copper Plated through Holes on Thermomechanical Reliability** Janine Conrad, Technische Universität Berlin **The Impact of Processing Conditions on Bond Reliability in Pressureless Silver Sintering** Rajrupa Paul, Hitachi Energy Ltd.	**Session 3D** Makalu ► Assembly and Manufacturing **A New Carrier Tape for Direct Transfer Bonding (DTB) Process with Ultra-thin Chips** Tomoka Kirihata, Lintec Corp **Ultra-precise Dispensing for High-resolution Redistribution Layers and 3D Interconnects in Advanced Packaging Applications** Priot Kowalczewski, XTPL SA **Microelectronic Packaging Challenges for Stacked Superconducting Qubit Chips Using Indium Bump Bonding** Andreas Schneider, STFC-RAL	4:35pm 5:50pm
		6:00pm 7:30pm

Wednesday September 17th

9:00am 9:45am	**Keynote 4►**	Recent Trends in Automotive Power Module Designs and Technology for Traction Inverters
9:45am 10:30am	**Keynote 5►**	System Technology Co-optimization for Advanced 3D & Heterogeneous Integration

Break – Posters – Exhibition

11:15am	**Session 4A** Auditorium ► Assembly and Manufacturing	**Session 4B** Kilimandjaro ► Design, Modelling and Simulation
	In-situ Plasma Monitoring Study for Wire Bonding Process Improvements Nohora Caicedo, STMicroelectronics	**Intelligent Prediction of Warpage in Molded fcBGA Packages: An Optimization and Modeling Approach** Jean-François Sauty, ASE Europe
	Impact and Control of Residual Stress in Ceramic Packages Markus Eberstein, ASML Berlin	**Comparative FEA Analysis of Cu Clip and Al Wire Bonding in Power Discrete Packages** Sung-Uk Zhang, Dong-Eui University
	Wafer dicing technique for close-butted assemblies Sarah Renault, CEA	**Investigation of thermal performance of various thermal interface materials used in top-side-cooled MOSFETs** Kshitij Anil Kolas, Fraunhofer Institute
12:30pm		

Lunch Break – Posters – Exhibition

1:50pm	**Session 5A** Auditorium ► Substrate Technologies	**Session 5B** Kilimandjaro ► Optoelectronics
	Approach for Extracting the Relative Permittivity of Sol-gel Using a Ring Resonator Fabricated on an LTCC Substrate Achraf Sadeddine, IMT Atlantique	**Precise Alignment and Laser-assisted Bonding of Multichannel Laser Diode Chips for Silicon Photonics Integration** Aleksandr Vlasov, Optoelectronics Research Centre
	Insulation Layers on Copper Surfaces of Ceramic Circuit Boards for Smart Power Modules Claudia Feller, Fraunhofer Institute	**Assembly Perspectives on Flip-chip Integration of 1x, 4x and 8x Array InP-SiN Hybrid Laser Devices to Si Photonics Wafers with Sub-500 nm Misalignment** Damien Leech, Imec
	Optimized Castellated Hole Interconnects for Ceramic-based Modular Millimeter-Wave Applications up to 85 GHz Paul Perlwitz, Christian Tschoban, Uwe Krieger, Qaisar Khushi Muhammad, Harald Pötter, Martin Schneider-Ramelow, Fraunhofer IZM	**Impact of TSV Mechanical Stress on Silicon Wave-guides Using Phase Shift Interferometry** Jean Charbonnier, CEA-Leti
	Glasses as substrates for packaging: Remarks on mechanic reliability. Martin Letz, Schott AG	**Package and Process Development of Molded Image Sensor Package** Alastair Attard, UTAC Group
3:30pm		

Dr. Uwe Hansen, VP Power Component Development, Bosch Auditorium	9:00am 9:45am
Sébastien Dauvé, CEO, CEA-Leti Auditorium	9:45am 10:30am

Session 4C Mont Blanc ► IC Packaging **Impact of PFAS Removal on the Harsh Environment Reliability of Semiconductor Packaging** Pradeep Lall, Auburn University **FC-LGA for Power Devices: Peculiarities and Challenges Compared with Digital Products** Stefano Cacciamani, STMicroelectronics **Modular Integration of Sensor-Chiplets using Rapid Prototyping including Interconnects and Protective Waveguide Packaging** Severin Schweiger, Fraunhofer Institute	**Session 4D** Makalu ► Poster Session #1 **Session Chair: Oliver Krammer, Budapest University of Technology and Economics**	11:15am 12:30pm

Session 5C Mont Blanc ► Emerging Technologies **TBM-free Plasma Etch Die Singulation** Partia Naghibi, HRL Laboratories **Anti-counterfeit Semiconductor Package Using a Unique Identification Mark** Ken Takano, Lintec Corp. **Metal Oxide Reduction Using Inline Openair-plasma Process to Enhance Adhesion and Improve Durability in Electronics** Dhia Bensalem, Plasmatreat GmbH **Surface Conditioning of LTCC Substrates for Improved RF Signal Propagation** Norayr Nessimian, TU Ilmenau	**Session 5D** Makalu ► Poster Session #2 **Session Chair: Stoyan Stoyanov, University of Greenwich**	1:50pm 3:30pm

	Break – Posters – Exhibition

4:05pm	**Session 6A** Auditorium ► System in Package	**Session 6B** Kilimandjaro ► Quality and Reliability
	Highly Integrated Low Power Wireless Sensor Node Luca Maggi, STMicroelectronics **Advancing Fan-Out Wafer-Level Packaging for III-V/CMOS Optoelectronic Transceiver SiP Integration** Perceval Coudrain, CEA-Leti **RF Characterization of Microscale Transmission Lines on Polymer-based Silicon Interposers for HPC Applications** Alexander Gaebler, Fraunhofer IZM	**Advanced Defects Repair Techniques for Enhancing Yield in Packaging Architectures** Dmitri Burshtyn, KL **Prognostics and Health Monitoring: Case Study of a Light Rail Vehicle Power Converter Assembly** Mike Roellig, Fraunhofer IKTS **Optimizing Ag Paste Thickness for Reliable Power Module Packaging** Ran Liu, Osaka University, Japan
5:20pm		
5:30pm	Bus transfer: Busses leaving venue for conference dinner	
7:00pm 10:00pm	Conference Dinner	

Thursday September 18th

8:45am 9:30am	**Keynote 6►** Advanced Packaging – The Key Technology for Chiplet Integration
	Room Change

9:40am	**Session 7A** Auditorium ► Smart Manufacturing	**Session 7B** Kilimandjaro ► IC Packaging
	Process Development for Cu Metallization on SiC MOSFETs with Inkjet Printing Technology Xiaojie Tian, Robert Bosch GmbH **Development of a Novel Pure-ag-sintering Paste for a Jet-dispensing Process to Achieve Highest Possible Conductivity for Miniaturized Electronic Components with a Pressure-less Sintering Process** Battist Rábay, Nano-Join **Additive Manufacturing of High-Performance Ceramics for Fabricating Single- and Multi-Material Components** Martin Schwentenwein, Lithoz	**"Advanced Packaging" — A must for the Next-Gen AI and HPC Hardware ! And not Only !** M.Bilal Hachemi, Yole Group **Advancing IC Substrate Manufacturing: Overcoming Challenges and Exploring Opportunities with 10µm Line/Space Technology** Stephan Trautweiler, GS Swiss PCB **Heterogeneous Integration and Wafer-level Packaging by Micro-transfer-printing** Sebastian Wicht, X-FAB MEMS Foundry
10:55am		
	Break – Exhibition	

Session 6C Mont Blanc ► Materials **Ag-nodule Mediated Bonding Using Liquid Quenched Ag-Si Alloy** Koji S. Nakayama, Osaka University **Thermal Characterization of Electrically Conductive Adhesives and Pressureless Sinter Pastes – Comparison of Data Sheet and Real Application** Antje Steller, Baker Hughes Inteq GmbH **Characterisation and Modelling of Sintered Joints Used in Power Electronics** Laurent Vivet, Valeo		4:05pm 5:20pm
		5:30pm
		7:00pm 10:00pm

Prof. Dr.-Ing. Ulrike Ganesh, Managing Director, Fraunhofer IZM Auditorium	8:45am 9:30am

Session 7C Mont Blanc ► Interconnection Technologies **Key Technologies and Design Aspects for Advanced FOCoS Packaging** Po-An Li, Advanced Semiconductor Engineering **A Novel Photo-patternable Epoxy Flux Material for A New Horizon in Fine Pitch Flip-chip Interconnections** Gwang-Mun Choi, Electronics and Telecommunications Research Institute **Integration Technology Development of Chip-Antenna Interface for Short Range mmWave Wireless Communication** Ran Yin, Institute of Electronic Packaging Technology	**Session 7D** Makalu ► Inspection and Test **Visualizing Vibrations of Electronic Modules in Test** Artem Ivanov, Landshut University of Applied Sciences **Lensless Through-silicon Microscopy System for Precise Alignment in Photonic Integration Processes** Aleksandr Vlasov, Optoelectronic Research Centre **Investigating the Role of Thermal Effects in RF Immunity of MEMS Microphones** Margarita Chizh, Department of Electrical Engineering, Munich University of Applied Sciences	9:40am 10:55am

11:30am	**Session 8A** ► Materials — Auditorium	**Session 8B** ► Assembly and Manufacturing — Kilimandjaro
	Understanding Solder Creepage in Thin Si Devices Through Advanced Traceability Systems Chaimaa El Mazyani, STMicroelectronics	**High density 3D interconnections for high performance CdTe based X-rays detectors** Jean-Michel Guinet, 3D PLUS
	Enhancing the Reliability of Harsh Environment Electronics Through PFAS-free Multilayer ALD + Parylene Coatings Rakesh Kumar, Specialty Coating Systems, Inc.	**Atmospheric Plasma Cleaning of Copper Oxide and Tin Oxide for Flux-Free Interconnect Bonding** Daniel Pascual, Ontos Equipment Systems
	Insulation Materials for Advanced Packaging Applications Reki Nakano, Ajinomoto Co., Inc.	**A single step process for Die-attach and substrate-attach with pressure assisted sintering to face harsh conditions** Anne-Marie Laügt, Inventec Preformance Chemicals
12:45pm		

Lunch – Exhibition

2:00pm 2:45pm	**Keynote 7►** Charting a Path for the Chiplet Era and Beyond
2:45pm 3:15pm	**Awards and Closing** — Auditorium

Session 8C Mont Blanc ► Power Electronics **Measurements at High Temperature for Thermal Resistance of MOSFETs** Corina Ruxandra Mitulescu, Norocel Codreanu, Ciprian Ionescu, Paul Svasta, Mihai Branzei National University of Science and Technology POLITEHNICA **Influence of Uneven Chip Solder Layer Thickness on the Reliability of Power Modules** Aylin Aksoy, Siemens AG **Reliability Evaluation of Direct Bonding for SiC Power Devices by Power Cycling Test** Marius Köhler, Hamm-Lippstadt University of Applied Sciences		11:30am 12:45pm

Craig Bishop, Chief Technology Officer, Deca Technologies Auditorium	2:00pm 2:45pm
	2:45pm 3:15pm

Access to program online

Social Event

▸ **Château Sassenage**

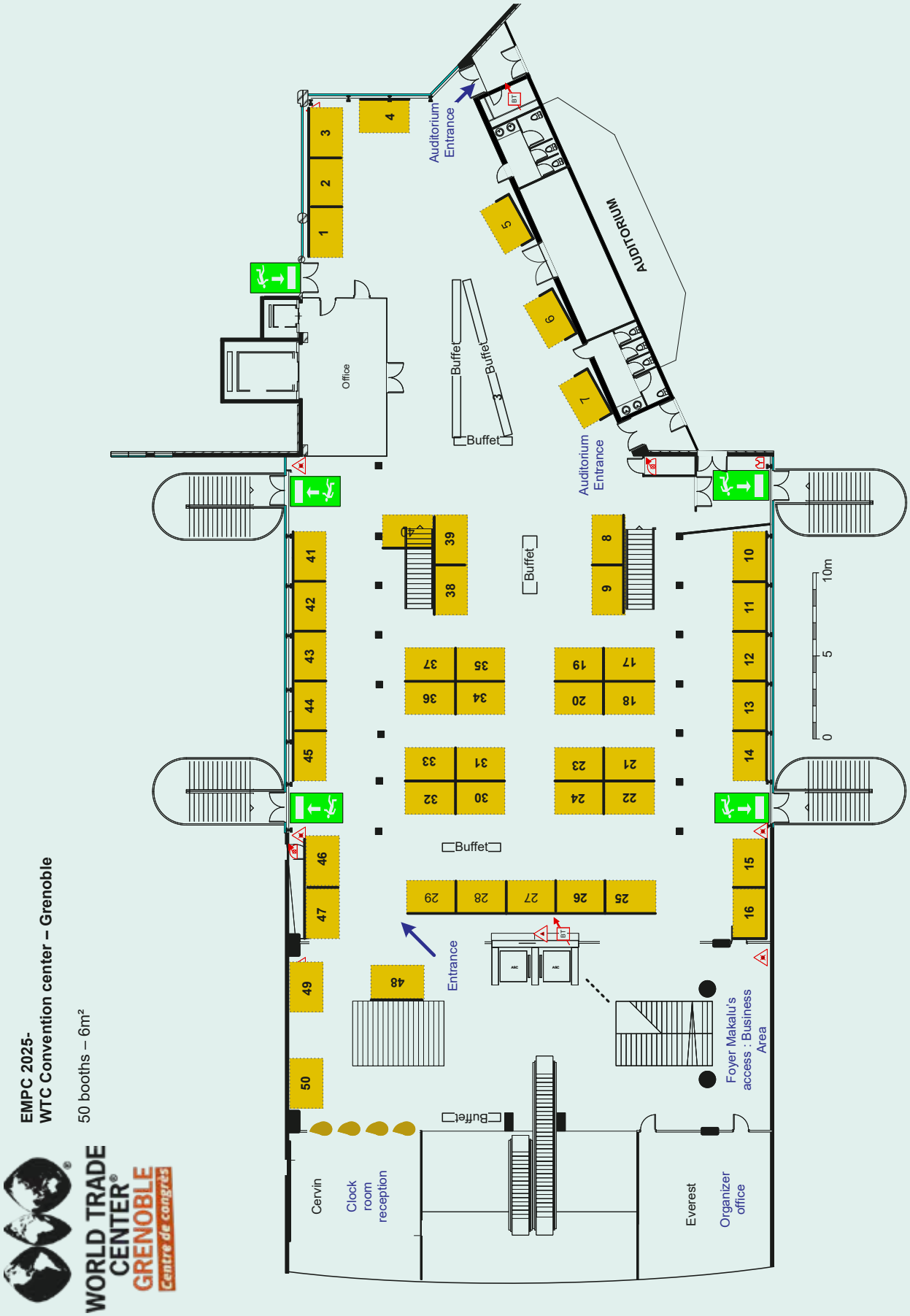
Transportation by Perraud Bus from WTC
(30 minutes)
17h30 first departure
17h45 second departure
18h00 third departure

▸ **Social event program**
18h00 - 19h00 Visit inside Castle
(20 minutes)
18h15 - 19h30 Appetizers & Music
19h30 - 22h15 Dinner

Return to WTC by Perraud Bus
transportation (duration: 20 minutes)
22h15 first departure
22h30 second departure
22h45 third departure

▸ **Sponsors**

Exhibition Map



Exhibitors List

Page	Exhibitors	Booth
42	Group ACB	10
43	Accelonix	17
44	AEMtec	36
45	Alter Technology	11
46	Amadyne	44
47	ASE, Inc.	27
48	Besi	37
49	Caplinq Europe	45
50	CDS Electronique	26
51	CEA-Leti	4
52	Chimie Tech Service	20
53	DELO Industrial Adhesives	47
54	Desire4EU	12
55	Dyconex	29
56	Egide	8
57	Electron Mec	24
58	Elematec Europe	25
59	Elemca	39
60	Eurofins MASER	2
61	Finetech	43
62	Fraunhofer IZM	49
63	GS Swiss PCB	35
64	HEF Group	34
65	Hybrid	38
66	iMAPS France	50
67	iNPACK	18

Page	Exhibitors	Booth
68	**ISP System**	32
69	**IST**	21
70	**I-TRONICS Pte**	13
71	**Kyocera**	6
72	**MB Électronique**	16
73	**Metronelec**	40
74	**Micronor**	9
75	**Microworld**	30
76	**Micro System Technologies**	46
77	**Murata**	28
78	**Nanotec International**	41
79	**ONTOS Equipment Systems**	19
80	**PacTech**	15

Page	Exhibitors	Booth
81	**Plasmatreat**	14
82	**Protavic International**	23
83	**Roartis**	42
84	**SERMA Microelectronics**	5
85	**SET**	7
86	**Synergie CAD PSC**	31
87	**Taipro Engineering**	33
88	**Teledyne e2v**	22
89	**UniTemp**	1
90	**Valtronic**	3
91	**Yole Group**	48

Group ACB

Booth 10

Activities

Group ACB is a PCB manufacturer based in Europe with 3 manufacturing sites (2 in France, Atlantec & Cibel and one in Belgium ACB). We are focus on high technology and high reliability PCB.
We can support quick turn over manufacturing (QTA) in many technologies such as Rigid, HDI, Flex-Rigid, Sequential, Flex-Rigid HDI, Thermal management, RF and HF.
We are also specialist on PCB for the Semiconductor market; we can support all kind of applications with thin tracks and gaps made with organic PCB technology

Products

From ATE Loadboards (for wafer or final test) to evaluation boards for customer, ACB can also supply your HAST and HTOL reliability boards.
Main characteristics are 6,4 mm thick PCB , dimensions 600x700 mm , large drill aspect ratio, inhouse plating for reliable contacting, laser drill, last generation etching process for thin and controlled impedances lines, and induction press.
ACB is also qualified by ATE manufacturing companies for hyper and RF PCB.
Consistently new released substrates offer to customer to reach stretched test performances.
Time to market oriented organization with QTA (Quick Turn Offer) fab for very high demanded customers.

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Accelonix

Booth 17

Activities

Accelonix is a solutions provider of equipment, materials and software for electronic & micro-electronics assembly. Accelonix group focus is western Europe, for industrial and research institutions, working in all sectors of the electronics industry.
Our service is based on close partnership with all Accelonix suppliers, through exclusive agreements in combination with in-house technical team, permuting rapid and efficient customer services and technical support.
Our success is built on an attitude for « innovation & opportunity » in synergy with a mix of complementary products and technologies. It is our intention that our customers benefit directly from this synergy, in addition to our contact and experience base, built up from over 25 years existence of Accelonix, and many decades of industrial experience for those in the company.
In addition to activities in Micro-assembly, Accelonix France is also active in the domains SMD pcb assembly and test, and Hi-rel component supply.

Product

- dicing – wafer, glass, ceramic, composite
- dispensing & jetting – pumps and machine for glue, solder, glob top, underfill,
- die attach and die sorting: MCM, Hybrid, silver glass, flip chip, eutectic
- wire bonders: manual & Automatic; fine & heavy; wedge & ball
- Battery bonding (Wirebonding, Smartwelding, Laserwelding)
- back-end plasma process – batch, on-line for wirebond and surface treatment
- vacuum pressure furnace – low void, flux free solder & brazing & wafer bonding
- hermetic sealing – seam sealing
- clean room & dry cabinets – modular and integrated solutions
- modular bond test – pull, shear, flex, stud pull
- screen printing – for ceramic substrates

Equipment for Metrology

- Non-surface contact profilometry
- Themal warpage metrology

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AEMtec

Booth 36

Activities

AEMtec is one of the global acting specialists for the development and production of a variety of precision optoelectronic products. The wide technology portfolio and outstanding services in the area of miniaturization mean reliable solutions like components, modules and complete systems.
The motivation is not only to drive innovations but also to accompany the customer along the entire value chain.
Our customer-specific products are complex electronic assemblies with precise component placement requirements. In a cleanroom environment (ISO 5-8) AEMtec offers a unique spectrum of high-end chip level technologies. AEMtec is ISO 9001, ISO 13485 (Medical) and ISO 14001 (Environmental) certified.

Product description

Wafer Back-End Services (UBM, SBA, Dicing), Chip on Board and SMT Technologies, optical components, VCSEL Photodiodes, MEMS, Moded Optical Interfaces and System Integration Packaging.

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Alter Technology

Activities

Alter Technology is a European company providing Outsourced Semiconductor Assembly and Test services of microelectronic semiconductor devices such as ICs, ASICs, MEMS, sensors, laser diodes, LEDs, VCSELs and discretes. We offer a complete back-end turn-key solution from wafer processing, package design, assembly, testing to fully qualified products ready to be commercialized.

Alter Technology's European capabilities and proximity allow customers to reach faster time-to-market by reducing lead times and increasing product development. We act as a single point of contact with full traceability in our processes and accountable for the quality of our services. Through our group of companies in Spain, UK, France and Germany we guarantee a fully independent European production, making us a key player to achieve and secure national and European dependency for sensitive sectors such as communications, military, defense, aerospace and quantum among others.

Products

Our expertise in semiconductor solutions spans the full product life-cycle: from design through prototyping, process optimization and production. Some of our services includes:

- Wafer back-end processing
- Packaging & Assembly
- Electrical Wafer Sort & Final test
- Qualification, Reliability, counterfeit and Failure Analysis
- Fast-turn IC Assembly & Prototyping (5-7 days turnaround)
- Long-term Storage – Globally unique TAB® long-term conservation process for the long-term storage of electronic components for up to 50 years
- Automated volume manufacturing

Booth 11

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Amadyne

Booth 44

Activities

Amadyne founded in 2000 is located in Bühl in the Rhine valley near Baden Baden from where the company offers direct support to the German speaking countries. In other countries Amadyne is represented by selected dealers. Amadyne offers compact, flexible solutions for the automation of microelectronic assembly manufacturing. Our systems provide for the precise production of sophisticated and complex components for micro systems engineering, micro opto-electronics and micro mechanical assemblies suitable for :

- small-medium-large production batches
- standard and advanced packaging processes
- complex high mix & high quality products
- integration of customer specific solutions
- short setup times
- fast product changeover

Product

Amadyne's current product portfolio includes the CATII and fab platforms.

▸ **CATII platform:**
The CATII is an automatic Micro Assembly System for picking and placing of components from various presentation formats, as well as for applying adhesives. Currently there are two versions from the CATII available called CATII and CATIIL with different working areas. Both systems use AMADYNE's advanced software platform with its fully developed process capabilities. The system is quick to program and simple to operate for the assembly of products within the microsystems industry.

▸ **fab platform:**
The fab is a compact, flexible automatic assembly platform for handling virtually any kind and size of component, as well as for applying adhesives. Typical applications are pick & place, dispensing, sorting, inspection and test functions. Currently there are two versions from the fab available called fab1 and fab2. Both systems uses the latest hardware technology, combined with a network transparent fully graphical control software, interacting with an SQL server based backend.

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ASE, Inc.

Activities

ASE, Inc. is the leading global provider of semiconductor manufacturing services in assembly and test. In a world that runs on semiconductor technology to achieve lifestyle, efficiency and sustainability goals, packaging innovation is at the heart of what ASE does. Today, ASE is delivering on the promise of heterogeneous integration, through advanced packaging, system-in-package, and chiplet solutions to meet growth momentum across HPC, Automotive, AI, 5G, and more.

Portfolio

The Company develops and offers complete turnkey solutions covering IC packaging, design and production of interconnect materials, front-end engineering test, wafer probing and final test, as well as electronic manufacturing services through USI, Inc. To learn about our technology advances and our VIPack™ platform, designed to enable vertically integrated package solutions, please contact your regional ASE office, visit aseglobal.com or follow us on LinkedIn.

Booth 27

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Besi

Booth 37

Activities

Besi is a leading supplier of semiconductor assembly equipment for the global semiconductor and electronics industries offering high levels of accuracy, productivity and reliability at a low cost of ownership. Besi develops leading edge assembly processes and equipment for leadframe, substrate and wafer level packaging applications in a wide range of end-user markets including electronics, mobile internet, cloud server, computing, automotive, industrial, LED and solar energy. Customers are primarily leading semiconductor manufacturers, assembly subcontractors and electronics and industrial companies. Besi's ordinary shares are listed on Euronext Amsterdam (symbol: BESI), its Level 1 ADRs are listed on the OTC markets (symbol: BESIY) and its headquarters are located in Duiven, the Netherlands.

Product

▸ **Die Attach**

Besi offers a wide range of die attach systems based on leading-edge technology.

▸ **Packaging**

Besi's Packaging product group designs, develops and manufactures molding, trim & form and singulation systems under the Fico brand name.

▸ **Plating & Cleaning**

Meco manufactures and supplies continuous plating and leadframe cleaning systems to suit the electronics industry.

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Caplinq Europe

Booth 45

Activities

Caplinq is a global, technology-driven company specializing in the development and distribution of advanced materials for the semiconductor, electronics, automotive, and energy industries. As a fabless manufacturer, Caplinq bridges the gap between innovation and application by offering high-performance specialty chemicals, adhesives, and engineered plastics tailored for high-tech manufacturing environments.

Product

Caplinq offers a comprehensive portfolio of advanced materials designed to enhance performance, reliability, and sustainability in microelectronics and packaging but also renewable applications.
Our product categories span critical stages of semiconductor and electronic assembly, like:

- **Die Attach Materials:** Henkel's Electrically and thermally conductive adhesives and pastes, optimized for high power, high temperature, and automotive-grade applications.
- **Wafer Processing Materials:** Wafer-level encapsulants and also dielectrics, and temporary bonding adhesives for advanced packaging and 3D integration.
- **Printable Inks & Shielding Materials:** Designed for EMI shielding, flexible conductive pathways and dielectrics, these HENKEL coatings and inks improve signal integrity in dense electronic assemblies.
- **Molding Compounds:** Hysol and LINQ Epoxy molding compounds for semiconductor and power electronics, including green, halogen-free, and high-thermal conductivity variants for high power devices.
- **Liquid Encapsulants & Underfills:** Capillary underfills, glob tops, and dam-and-fill systems designed for flip-chip, CSP, and BGA applications—offering improved thermal cycling reliability, mechanical reinforcement, and protection from moisture and contaminants.
- **Thermal Interface Materials (TIMs):** Honeywell's Phase change materials, thermally conductive pads, and pastes to reduce junction temperatures and enhance device lifespan.

We collaborate closely with our customers, leveraging our extensive network and knowledge to deliver tailored solutions that meet your application needs. In addition to our LINQ products, we are proud official Global distributors of HENKEL, Honeywell, Hysol, DMI, Polar performance materials, Bostik, JNC and Ionomr.

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caplinq-corporation

CDS Electronique

Booth 26

Activities

CDS Electronique distributes materials for micro-electronic manufacturing (packaging) and offers equipment for microdispensing and ink-jet printing. Do not hesitate to contact us, we can carry out tests from our showroom in Bussy-Saint-Martin (77).

Product

- Encapsulation- underfill resins NAMICS
- Conductive adhesive - (high thermal conductivity) NAMICS
- Die-attach NAMICS
- Nano-inks (silver , gold) XTPL
- Micro-dispensing solution MUSASHI Engineering
- Nano- dispensing expertise XTPL
- Impression ink-jet MICROCRAFT

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CEA-Leti

Booth 4

Activities

CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti pioneers micro-& nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 1,900, a portfolio of 3,100 patents, 11,000 sq. meters of cleanroom space and a clear IP policy, the institute is based in Grenoble, France, and has offices in Silicon Valley and Tokyo. CEA-Leti has launched 70 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

Product

CEA-Leti offers a wide range of packaging solutions and tailored developments for industrial partners:

- Fast data exchange technologies: High density 3D-IC, active interposers & advanced photonics
- Design technologies: Partitioning studies for best Power/Performance/Area/Cost trade-off & 3D CAD flow
- 3D integration and packaging technologies: TSV, routing, redistribution layers, connecting - µbumps, hybrid bonding
- Heterogeneous integration: Fan-out wafer lever packaging tailored for various applications and flex substrates for ultra-thin and conformable systems

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CEA-Leti

Chimie Tech Service

Booth 20

Activities

Chimie Tech Services (CCI Eurolam Group) is your partner for the supply of specialty materials and chemicals for the electronics industry. We are waiting for you in Grenoble to present the latest innovations for electronic design and manufacturing, including:

1. Latest generations of Indium Corporation materials, leading materials manufacturer of solders, fluxes, solders and thermal interface materials for the electronics and semiconductor assembly industry.
2. Microelectronics and semiconductor packaging: DuPont metallization solutions for UBM (underbump metallization), RDL, Cu pillars, as well as polymers and dielectrics for RDL. Photolithographic resins and solutions for developing, cleaning and etching thin layers.
3. The latest substrates for circuit boards to meet microwave, low loss requirements, as well as high performance and high temperature substrates, and also the “IC substrates” from the EMC range.
4. Micromax functional inks and substrates for printed electronics (heating, stretchable, thermoformable inks, PI resistive inks, etc.) meeting new specifications in terms of low temperature baking, dispensability, fine resolutions and improved chemical resistance

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DELO Industrial Adhesives

Booth 47

Description

DELO is a leading manufacturer of high-tech adhesives and other multifunctional materials as well as adhesive dispensing and curing technology. Its products are mainly used in the semiconductor, automotive, and consumer electronics industries. They can be found in almost every mobile phone and in most cars worldwide, for example in cameras, loudspeakers, electric motors, or sensors. Customers include Bosch, Huawei, Mercedes-Benz, Osram, Siemens, and Sony. DELO's headquarters are in Windach, Germany, near Munich, with subsidiaries in China, Japan, Malaysia, Singapore, and USA, as well as representative offices and distributors in numerous other countries. The company employs a workforce of 1,160 staff and achieved revenues of €245 million in the last fiscal year.

Product

DELOs semiconductor packaging materials are suitable for a wide range of applications, such as die attach or reinforcement in board and package level applications via underfill, corner fill or edge bond. The protection of bare semiconductor chips and their wires is another important application, for which DELO provides ultra-low CTE materials that also offer the option to be cured just by UV-light. Latest developments include adhesives like DELO DUALBOND EG6290 – a material for CMOS image sensor packaging, with which the filter glasses can be bonded directly to the die. It can be dispensed in narrow, high bondlines, can compensate for temperature-dependent pressure changes, and meets the requirements of typical automotive standards like AEC Q100. DELO DUALBOND EG4797, on the other hand, is a newly developed product to solve spatial constraints. With this adhesive, micro structures with line widths smaller than 100 µm and aspect ratios greater than 5 can be dispensed before UV light curing in one step takes place. These micro dams can, e.g., serve as a flow stop for underfills or function as a light barrier in optical sensors. Overall, many of our high-tech solutions unlock new possibilities in the field of advanced packaging and thus make a significant contribution to further miniaturization, like our solutions for CPU & GPU packaging.

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Desire4EU

Booth 12

DESIgning & REcycling
sustainable Electronic boards for EUropean circular economy

Activities

DESIRE4EU will be a pioneer of sustainable electronics through fully circular bio-based printed circuit boards Driven by the goal of revolutionising the electronics industry, the DESIRE4EU project is set to launch a new era of sustainability with the development of fully circular, bio-based printed circuit boards (PCBs). Indeed, DESIRE4EU's innovative approach focuses on creating PCBs that are not only industrially credible but also environmentally friendly. The project plans to incorporate bio-based and biodegradable materials to significantly cut down on harmful waste and improve the recovery of critical metals like copper by 2030.
We aim to develop:

- new eco-design rules able to maintain the overall performance of the electronic circuits while maximizing the circularity of the boards,
- new dielectric materials compliant with most of the criteria of IPC standards
- bio-based PCB protection products to slow down its bio-degradation in ambient conditions and eco-friendly assembly processes.

Product

We will present at our booth:

- raw, unengraved bio-based candidate substrate for PCB fabrication that is sustainable and scalable, capable of supporting multi-layer designs compatible with modern component packages : double sided, in between, full laminates, coated versions....
- demonstration cards, test samples at the different stage of PCB assembly production (bare laminate, patterned laminate, assembled PCB).
- demonstration Arduino boards based on the Arduino Nano and Arduino Uno designs
- sample of conformal coating as example of the solvent used in the environmentally friendly and time-efficient bioleaching process

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Dyconex

Booth 29

Activities

DYCONEX is committed to delivering the highest quality products in the industry – and we back this promise with a deep-rooted expertise in advanced interconnect solutions for medical applications. Our success in the field of high-reliability PCBs is built on multiple strengths: a customer-driven development and design process, decades of experience in low-volume, high-mix manufacturing, and a sharp focus on the most demanding segment of the industry – IPC Class III for medical devices.
What truly distinguishes us is our unwavering dedication to quality, precision, and innovation. We continuously invest in next-generation technologies, particularly in the areas of miniaturization, high-density interconnects, ultra-thin substrates, and advanced via structures. These capabilities are essential for today's and tomorrow's medical devices – from active implants and wearable systems to diagnostics and neurostimulation.
We work in close collaboration with our customers from concept to production, enabling tailor-made solutions that address specific technical, regulatory, and clinical requirements. This integrated approach not only ensures product performance but also supports our partners in accelerating their time to market.

Product

DYCONEX products stand for highest precision, reliability, and technological excellence – specifically designed for demanding applications in the medical field. Our portfolio includes a wide range of highly complex PCB solutions such as HDI and substrate technologies, ultra-thin flex and rigid-flex circuits, special builds with microstructured surfaces, and multilayer designs with features as fine as 10 µm lines/spaces.
Our products are used wherever uncompromising quality is essential – including active implants, audiological devices, neurotechnology systems, portable therapy solutions, ultrasound applications, in-vitro diagnostics, and minimally invasive surgical instruments. They meet the highest standards in biocompatibility, mechanical stability, electrical performance, and long-term reliability – even under extreme conditions.
We process a wide range of high-performance materials including engineered polymers, copper-clad laminates, ceramics, and thin-film metals – all tailored to the specific requirements of the application. Our offering is complemented by services such as laser drilling, microstructuring, selective metallization, and integrated testing and verification solutions to support our customers throughout the product lifecycle.
Thanks to our many years of experience and a fully controlled manufacturing process, we are able to respond flexibly to individual requirements – whether for high-precision prototypes, complex low-volume series, or demanding full-scale production. All products undergo rigorous quality checks and comply with international standards such as ISO 13485, IPC Class III, and customer-specific specifications.

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Egide

Booth 8

Activities

The Egide Group is an international company specialized in the design and manufacturing of hermetic packages for sensitive electronic and optronic components. Our core expertise lies in ceramic packaging, glass-to-metal and ceramic-to-metal sealing, thermal management and special metal alloy processing.
Egide serves critical industry segments like aerospace, defense, security and energy.
The group operates manufacturing facilities in France and the United States.
Egide offers engineering services for custom packaging designs and advanced materials. Our solutions meet stringent requirements for hermeticity, thermal management, reliability, and high-temperature or radiation-hardened applications.
With decades of experience, Egide is a recognized leader in the hermetic packaging market, enabling high-performance and mission-critical systems worldwide.

Product

Hermetic packaging design and manufacturing for sensitive electronic and optronic components.

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Electron Mec

Activities

Electron Mec is committed to providing world best in class tools, processes and services to High-Tech players in Europe, meeting and exceeding the requirements of its customers. Based in France, Italy, Germany, Switzerland and Spain we support our partners locally relying on process knowledge and experience.

Product

Electron Mec will be presenting a series of High-Tech products including:

- Controlled Atmosphere and Vacuum solder Reflow Ovens - ATV and DESPATCH
- Plasma Surface Treatment and etching – PVA TEPLA, PANASONIC and SAMCO
- Mask and Maskless Photolithography equipment – SUSS and NANOSYSEM
- Coating and Dispensing systems – MUSASHI, SUSS and HUMMINK
- Machine Vision Systems for Smart Automation and Inspection – MVP, VISIOROBOTICS, TORAY
- Laser Welding Systems for Ermetic Sealing – PYRAMID ENGINEERING
- PVD, CVD, PECVD Deposition technology – NANOVAK, POLYTEKNIK, SAMCO, KANEMATSU
- Hermetic Lids, Boxes and micro-machined parts - SURON
- Wet-Chemical Benches
- Bonding Technology – SUSS and TORAY
- Gloveboxes – KOREA KYION
- Customized PCBs – ELECTRON MEC
- PogoPins and Sockets – INDEPENDENT
- Temperature Control – CORREGE

Booth 24

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Elematec Europe

Booth 25

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Activities

Elematec Corporation is an integrated service company created in 1947, and since then we have continued to grow while wielding flexibility and speed to earn the trust of customers in the fast-evolving electronics industry. As a partner in manufacturing, we align ourselves with customers from the starting line of product development and work together with them to realize one-stop solutions by being involved from the planning and development stage. From there, we support them through the design, prototyping, and mass production stages. Through our industry-leading network in Japan and overseas (totalling over 70 branches) and over 7000 partners world-wide, we deliver products from electronic materials, parts and module products to finished products, on a global scale. We are happy to provide you a solution or missing item(s) in your BOM.

Product

Ceramic Packages: Through our cooperation with NTK Ceramic (Niterra Group), we offer fully customized multi-layer ceramic packages for chip encapsulation in complex applications (MEMS, Hi-Rel, Power, RF, Automotive, Image Sensors, etc.). These ceramic substrates can accommodate larger sizes and finer patterns, while also integrating solutions like Cu-based heat slugs and AlN for improved heat dissipation.
As a set solution for packaging, we provide:

- LIDs and CAPs for sealing, TO-CANs
- Cover glass lids and protective films, for image sensors

In general, for semiconductor manufacturing, processing and handling:

- Chemical products for manufacturing; adhesives, etc., Thermal solutions (TEC, TIM, heat dissipation materials, solutions also for IGBT)
- Tapes; dicing blades, wafer shipping cases and wafer rings, and other products for handling.

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Elemca

Activities

ELEMCA provides Lab services to understand and improve your electronic technologies, from wafer to component and assemblies :

▸ **Failure & construction analysis**
Computed tomography (3D X-Ray), Lock-in thermography, PHEMOS
FIB, SEM/TEM-EDX

▸ **Reliability**
Environmental testing (thermal cycling / shocks, climatic)
Digital simulation

Portfolio (semiconductor): LYNRED, MURATA, RAKON, TE, TDK/TRONICS, TELEDYNE-E2V

Booth 39

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Eurofins MASER

Booth 2

Activities

Eurofins MASER is an independent engineering service company. Since 1993 we have offered Reliability Test and Failure Analysis Services to the semiconductor and electronic systems industry.
We offer a wide range of qualification procedures (AEC Q100/JEDEC/MIL/IEC) to qualify your products according to the latest international standards or to your specific requirements.
Our state-of-the-art Failure Analysis laboratory will fulfill all F/A needs of our customers (Non-destructive analysis/construction analysis/FIB-CE/IPC inspection/ Advanced Failure Analysis).
Whether your company is active as Fabless Semiconductor Manufacturer, IC Design House, Electronic Manufacturing Service (EMS) Provider or Original Equipment Manufacturer (OEM) we can support you with your daily Reliability Test or Failure Analysis challenges.

Product

Independent service provider for failure analysis and reliability test on semiconductor- and electronic systems companies

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Finetech

Booth 43

finetech

Activities

Finetech is dedicated in developing equipment for micro-assembly, die bonding, die attach, flip-chip bonding with an accuracy from 0,3µm to a few µm. We target the industries of photonics, microelectronics, mems, medical devices and electronic rework.
Our machines are versatile and allow to realize all assembly processes, from eutectic to ultrasonic bonding, not forgetting epoxy glues and CAF. Of course sample preparation steps as formic acid dispense or plasma activation can also be done in the same easy to use process.
Finetech developped semi-auto tabletop equipment for prototyping and process development to fully automatized machines for volume production.
More information, tech papers and videos on our website: www.finetech.de
Looking forward to meeting you

Product

▸ Sub-Micron Table Top Die Bonder
The FINEPLACER® lambda 2 table top die bonding platform can be easily configured for a wide range of applications for process development or prototyping. Numerous process module options and in-field-retrofit capabilities guarantee maximum technological flexibility of the table top die bonder to protect your investment in the face of ever-changing challenges. Due to the table top flip chip bonder's ergonomic machine design and software-supported user guidance, the user remains at the center of action. Powerful optical systems allow the user to keep an overview at all times, even when working in the sub-micron range.

▸ Automatic Sub-Micron Bonder
The FINEPLACER® femto 2 is a fully-automated die bonder with 0.3 µ accuracy that offers unrivaled flexibility for prototyping & production environments The FINEPLACER® femto 2 can be configured and retrofitted at any time to support new applications and technologies. This makes this automatic flip chip bonder a perfect tool and reliable companion as applications migrate from product development to production

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Fraunhofer IZM

Booth 49

Activities

Research at Fraunhofer IZM means exploring and innovating application-driven, technologically advanced electronic systems and microsystems. The Institute believes in holistic system development that guarantees a long, reliable and functionally secure working life for electronic systems.
Chiplet assembly, hybrid bonding, Si interposer technologies, fan-out wafer level packaging (FOWLP), cryo-packaging, high-bandwidth memory (HBMs) integration, RF characterization, and packaging for 5G / 6G applications are just a selection of the many technologies and services from our portfolio that help advance the technologies of tomorrow.
Fraunhofer IZM, founded in 1993, has a staff of more than 400 and disposes of a lab area of over 8,000 sqm. About 80 percent of our turnover is earned through contract research.

Product

High-End Performance Packaging from Wafer to System: We envision the future of electronic packaging with a sense for all the requirements and capabilities already expected of smart electronic systems and their components - be they heat-resistant, long-lasting, custom-shaped, or even stretchable.
Traditional systems-on-chip that cram all of the features and functions of a microelectronic system onto a single piece of silicon are reaching the end of their potential in terms of performance, flexibility, and the design effort required. The need for further miniaturization and integration of more electronic functions into systems means that the performance standards expected today cannot be fulfilled.
The alternative: heterogeneous integration that combines different technologies in order to create miniaturized high-performance systems. Fraunhofer IZM has developed a range of heterogeneous integration processes, optimized for industry on production-ready high-end hardware.

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GS Swiss PCB

Booth 35

Activities

GS Swiss PCB AG is a specialist for highly miniaturized and reliable PCBs.
In volume production we manufacture substrates in standard technology with lines and spaces of 40 µm, substrate thicknesses down to 12 µm for flex and 30 µm for rigid PCBs and solder mask dam width of 30 µm. Copper filled stacked vias as well as copper filled through holes are standard processes and we offer final surfaces such as ENIG, ENEPIG, electrolytic gold, immersion silver and DIG.
With our sputtering machine for volume production we are able to manufacture PCBs in SAP-technology with lines and spaces down to 10 µm.
Our extensive testing capabilities include IST-testing, 3D topography measurement with submicron precision, analysis be electron microscope as well as ion cross section polishing.

Product

GS Swiss PCB AG excels in the manufacturing of highly miniaturized flex and rigid PCBs with lines and spaces down to 10 µm, cores of 12 µm for flex and 30 µm for rigid PCBs. Testing capabilities include IST-testing and 3D topography measurement. Our PCBs are used in hearing aids, medical implants and sensors as well as on Mars.

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HEF Group

Booth 34

Activities

The HEF Group, a global leader in surface materials engineering, offers its clients a comprehensive service ranging from research activities to process exploitation or component supply, including industrial development and technology transfer.
HEF's expertise in tribology, photonics, and hydrogen technologies is based on five areas of technical and material competence:

- Vacuum deposition and DLC materials
- Ion liquid nitriding
- Laser texturing
- Coated powders
- Friction components

Product

We are industrializing an innovative solution of Polymer Core Solder Balls (PCSB), enabling the creation of reliable and high-performance electronic component assemblies for various applications (aerospace, space, defense, mobility, etc.).
These solder balls offer three significant advantages:

- Increased resistance to thermomechanical stresses compared to standard solutions.
- Controlled standoff between the PCB and the BGA.
- 3D Assembly, Miniaturization
- Alternative to traditional non-collapsible lead solder balls
- Compatible with solder reflow according to IPC-J-STD-001

Polymer core solder balls help improving the lifespan of electrical contact for assembling BGAs on a printed circuit board

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HEF Group

Hybrid

Booth 38

Activities

With 30 years of existence, Hybrid SA is your Swiss partner for highly complex projects, from prototyping to serial production, from engineering to industrialization, with excellence driving every step of the process.
We will deploy our expertise in microelectronic assembly techniques like FlipChip, Wirebonding, 01005 size component automatic placement or Diebonding to help you bring your project to life.
We can also assist you with your routing and/or miniaturization layout design, component selection and innovative solution finding.
From medical to industrial, aero to consumer electronics, make sure that your project is in the best hands and contact us today, we will be thrilled to help you.

Product

µ Electronic Manufacturing Services

Application area: IOT (Internet of Things) - Datacom – Avionics – Scientifics – Imagery – Watchmaking – Industry – Medical - Security.

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IMAPS

Booth 50

IMAPS – International Microelectronics Assembly and Packaging Society – is a global community of microelectronic related engineers, scientists, manufacturers, end-users and supply chain companies. The Society aims to support the development and growth of the Microelectronics and related industries, and to aid the transfer of knowledge and information. This is achieved through networking, seminars, workshops, short courses, publications, webinars and websites. Members benefit from access to business networking and events at a reduced rate; technical information & receive society newsletters and other publications. IMAPS is the largest Microelectronic Packaging Society in the World!
IMAPS-France (French chapter) is a non-profit organization with 200 members from 110 companies or institutes in France.
IMAPS-France is one out of the 30 IMAPS chapters throughout the World. To that end, we organize events each year, in English language, these are namely: MiNaPAD, POWER, THERMAL.

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iNPACK

Activities

We go beyond design limits to offer you cutting edge semiconductor and electronics assembly, testing and IC package design including LGA, BGA and 2D & 3D customized solutions. Featuring fully supported automated processes, MW microelectronics assemblies, System-in-Package (SiP) & heterogeneous integration. We also offer high level expertise in organic substrate design and manufacturing based on advanced materials, subtractive and mSAP processes.

Miniaturization Technology:

- IC Packaging & System-in-Package (SiP) design, Semiconductor assemblies
- MW microelectronic assemblies, Organic substrates
- Process development & DFM processes

iNPACK Benefits:

- Time To Market (TTM), Design & manufacturing under one roof
- Cost effective solutions, Innovative approach
- Customization options, In-house capabilities: substrates, PCB, micro assembly

Product

▸ Advanced IC Packaging & Organic Substrates – All-in-One Solutions

We offer organic substrate expertise with high-density line/space width and advanced packaging that allows for a smaller form factor, increased functionality, high thermal conductivity, and improved process stability. System-in-Package (SiP) prototypes, or low/mid volume production, Multi-Chip-Modules (MCM), and more; all compatible with aerospace, defense, medical, and other top industry needs.

▸ Advanced Packaging Assembly

Our unique assembly process designs enable you to achieve high-level, customized results with IC packaging solutions tailor-made to your specific applications. Our customers are no longer bound by a specific design process dictated by individual fabricators or semiconductor packaging companies.

▸ Technological Edge

iNPACK are experts in organic substrates and enhanced micro-electronics packaging technologies, with cutting-edge capabilities that deliver complete, comprehensive substrate panel-level manufacturing and engineering support to our customers; in fact, they depend on it. We continuously work to improve interconnections between PCB, Substrate and Semiconductors through advanced technological know-how. Solutions include Organic Substrate materials, IC Substrates, Die Packaging, Multi-Chip-Module (MCM) technology, Chip Packaging and more. Creative solutions and enhanced design flexibility give us the ability to deliver high-speed, thermal and RF pathways that simplify integration processes, that improve overall system reliability.

Booth 18

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ISP System

Booth 32

Activities

ISP System has developed advanced features and capabilities to support specific Advanced Packaging Markets in the backend area. We enable customers to optimize the performance of their process in optoelectronics and photonics advanced packaging. Our dedicated team of highly experienced, creative technical and manufacturing professionals have collected more than 25 years of knowledge in advanced micro assembly solutions. We can provide you with both standard and customized equipment based on leading-edge technology.
Our team develops the systems with modern development tools focusing on:

- Concept development
- 3D construction
- Development of prototype systems
- Precision assembly
- Software development
- Customized machine controls
- Process vision systems
- Active alignment
- Image processing systems
- Process development and process production transfer
- Sampling and small volume production

Product

PHOTOMATIQ$_{TM}$
The newest generation of photonics micro-assembly and packaging equipment guarantees the highest degree of flexibility for the most demanding application: Laser DPSS, laser diode and stack, Lidar, PIC, Fiber Optical Connectors assembly.
The offering includes passive and active alignment process as well as glue dispensing and in situ UV curing.
Photomatiq™ is delivered with its own software: PHOTONSMART. PhotonSmart is an open control software, which allow non-automation experts to operate the machine, edit new recipes and supervise the production. Create your own manufacturing process with pre-developped function blocks using the pick and drop feature.
Learn more about Photomatiq™ on our website : www.isp-system.fr/products/photomatiq/

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IST

Activities

Founded in 1994, iST began its business from IC circuit debugging and modification and gradually expanded its scope of operations, including Failure Analysis, Reliability Assurance, Material Analysis and so on. iST has offered full-scope verification and analysis services to the IC engineering industry, its customers cover the whole spectrum of the electronics industry from IC design to end products. iST aims to expand its market presence in Europe. Beyond addressing customers' pain points, the company strives to offer innovative solutions to help clients work more efficiently and effectively.

Product

In response to the growing future trends, iST has established platforms for 5G/HPC/AI, Automotive Electronics verification, Space Satellite verification, Advanced Processes and Wide-bandgap Semiconductors, LTS (low-temperature soldering) Process verification platforms, as well as High-speed Transmission Signal Testing, offering comprehensive verification and analysis services. With a commitment to providing complete solutions to customers, iST has expanded its services beyond verification to encompass Wafer Backend Process for mass production service.

Booth 21

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I-TRONICS Pte

Booth 13

Activities

I-TRONICS Pte Ltd is the frontend application center located in Singapore that specializes in providing Design and Solutions for a complete range of electronic products such as:

- Microelectronic Packaging and its assembly
- Printed Circuit Board and its assembly
- Flexible Printed Circuit board and its assembly

Our team comprises of a highly competent technical core team who are the pioneers in the various electronic industry with more than 20 years of experience in design and manufacturing to meet competitive cost with the highest quality and reliability standard.

Product

Our offered services and products include:

- Design and layout of PCB/FPC/Substrates and its assembly.
- Provide full turnkey solution for Organic Substrates, such as PBGA / CSP / FCBGA and assembly.
- Provide full turnkey solution for Coreless Power Substrate and assembly.
- Provide full turnkey solution for IC packaging (leadframe base), such as leaded packages (QFP, SOIC, TSSOP, etc.) and unleaded packages (DFN, QFN, etc).
- Provide full turnkey solution for Wafer Bumping services such as Gold bumping, MCB, WLCSP, Cu RDL and Cu pillar, and its Final Test services.
- Perform SI/PI modeling and measurement during design stage.
- Provide full turnkey solution for Printed Circuit Board / Flexible Printed Circuit and assembly.

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Activities

High-reliability ceramic packages and substrates help to miniaturize components used in smartphones, fiber optics, automotive electronics (such as headlight LEDs), and a wide range of other applications. Materials, processing, and design technologies to ensure unparalleled substrate and package performance.
The rapid advancement of information and communications technologies (ICT) and the internet have fueled an extraordinary increase in the functionality and performance of electronic devices. Our organic packages help to support these developments.
Our other business domains extend to a wide range of industrial fields, such as digital equipment, automotive manufacturing, and energy, based on our organic material technology.

Kyocera

Booth 6

THE NEW VALUE FRONTIER

KYOCERA

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MB Électronique

Booth 16

Activities

MB Electronique, established in 1972, is a French company specializing in the sales of electronic test and measurement systems and equipment. We offer tailored design and the development of innovative testing solutions, as well as in-house testing services such as HALT/HASS and SAM. The company is committed to customer satisfaction by providing products from leading manufacturers, complemented by premium support and additional services. MB Electronique focuses its expertise in seven key areas: energy conversion, electronic test instrumentation, metrology, avionics testing, semiconductor testing, environmental simulation, and e-commerce. As of 2024, the company employs 65 people and reported a turnover of approximately €32 million.

Product

MB Electronique offers a range of equipment pertinent to the microelectronic & packaging market:

- Acoustic Microscopy: Non-destructive testing that utilize acoustic wave to inspect internal structures of electronic components, aiding in failure analysis and quality control.
- Probe stations: solutions for testing the semiconductor devices, enhancing efficiency and accuracy in quality assurance processes.
- Environmental Simulation Chambers: Equipment that subjects packaged components to controlled environmental conditions, such as temperature and humidity, to test their durability and reliability.
- Power Supplies and Loads: Equipment that provides controlled power to components during testing, as well as electronic loads to simulate various operating conditions.
- Die bonding / pick & place systems for components placement and sorting, using different technologies of soldering
- Wire bonding: electrical connection from die to package, using small Aluminum/gold wire (few µm diameter)

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Metronelec

Activities

Since 1975, Metronelec has specialized in the manufacture and sale of equipment for the electronics and microelectronics industries. Originally specialized in quality control, Metronelec has developed in the production area for several years and today offers a wide range that covers all processes from design to production.
In addition to the French parent company, Metronelec has branches in China, Tunisia and Morocco.
Metronelec equipment is marketed all over the world thanks to a large network of distributors trained to perform maintenance and local technical support.

Product

Manufacturer of solderability tester for components and ionic contamination analyzer
Distributor of equipment for the assembly of printed circuits online/offline and consumables for the electronics, optoelectronics and semiconductor industry in France
Main representations :

- NORDSON DAGE: multifunction bond tester system. X-RAY Systems
- SIKAMA: reflow ovens.
- FINETECH: Flip-chip bonders
- KOH YOUNG: 3D Paste Inspection systems and 3D AOI
- ITW EAE: screen printing systems

Booth 40

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metronelec

Micronor

Booth 9

Activities

More than 50 years as subcontractor expert in custom hermetic sealing & hermetic interconnections for harsh environment (pressure, intensity, tension, temperature, etc...)
Design and production of prototypes, small and medium series, based on customer technical specifications.
Small size of pieces (Ø 0,2 mm up to 150 mm)

- Glass to Metal seal (including dilver P1 (kovar) and titanium) and high and low temperature brazing (ceramic, sapphire, etc...)
- Base and precious metals electroplating (specific 99,99% pure gold for space applications)
- Hermeticity : Leak rate less than 10-8 mbar.l/s
- Electric isolation : Isolation resistance over 10 GΩ
- Breakdown voltage : from 500 to 3000 V
- Pressure : up to 3000 bars
- Operating temperature : from -180°C to +300°C (according to coating)

Precious metal electroplating processes (gold, silver) and common metal (tin, copper) for industrial applications (space, defense, etc...) – specific 99.99% pure gold electroplating process for space application

Product

Non exhaustive products list (based on customer's technical specifications) : feedthroughs, electronic packages, sensors, relay bases, connectors, isolators, igniters bases, medical implants, etc.

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Microworld

Activities

For more than 30 years, Microworld has become the essential partner of semiconductor and research actors. MW offers a complete range of equipments, accessories and consumables present at eachs steps of the process from Front-End to Back-End.
Our systems could be manual or semi-automatized in order to follow the products from R&D department to the industrialization.
In summary, if you have any questions concerning...

- Front-End characterization
- Failure Analysis / Probing
- Dicing
- Bonding
- Packaging
- And many others

... Come to meet us on Booth 30.
In addition, some of this equipments will be present to test it directly on your samples.
Don't hesitate any longer, we are waiting for you!

Product

Distributor and integrator for Semiconductor Industry.

Booth 30

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Microworld

Micro System Technologies

Booth 46

Activities

The Micro Systems Technologies (MST) Group provides innovative components and services for technologically advanced industries that demand miniaturization, exceptional performance, and the highest level of reliability. Examples are medical technology, aerospace & aviation, and challenging applications in telecommunications, industrial electronics, and sensor technology.

Active around the globe, the MST group consists of five technology companies with more than 1,100 employees in three countries, all of which offer their customers integrated solutions from conceptual design to series production.

The MST Group's quality system is derived from the stringent requirements of life-sustaining implants and ensures 100 % traceability of processes and materials. The companies are ISO 13485 and/or ISO 9001 and/or ISO 9100 certified.

For more information, please visit our virtual showroom: www.showroom.mst.com

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Murata

Activities

Murata Caen develops and produces high performances Capacitors on Silicon for demanding markets like medical, automotive, mobile, ultra-broad band or space applications. Silicon Capacitors are now an unmissable technology, and Murata leverages on more than 15 years of experience in this domain to offer best-in-class adapted products through a large and versatile portfolio, from standard capacitors to custom complex solutions for every single specific request.
Murata Caen is the perfect combination of an agile European semiconductor factory inside a large and powerful international company, leading the world of passive components.

Product

Silicon Capacitors are, as their name suggests, capacitors made from Silicon. The unique 3D nano structure made inside the Silicon offers two key benefits: on one hand, they present best-in-class electrical performances for applications up to 220GHz, with high stability over temperature, voltage (up to 1500V) or ageing; on the other hand, our customers can win the battle for integration thanks to the very high miniaturization and very low thickness of Silicon Capacitors.
Our products can be delivered as stand alone products, but also as capacitors arrays or even IPDs (Integrated Passive Devices).

Booth 28

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Nanotec International

Booth 41

nanotec international GmbH

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Nanotec international

Activities

Nanotec international provides solutions for semiconductor backend, assembly/packaging and related fields to the European market since around 25 years. Together with our strong partners (see below), we can supply equipment and materials for various processes: Wafer Bonding, Flip Chip and Die Bonding, Solder Ball and Cu Pillar Placing, Reflow, Sawing&Placement, Laser Marking, Laser Cutting, LED Sorting, Pick&Place Sorting, Void- Free Curing/ Soldering, Burn-In and many more. Our trained field service engineers, based all over Europe, are ready to assist on technical requests within a short time. Please contact us anytime to discuss your challenges and learn about the solutions and our new processes and products.

Product

Materials Equipment

- Burn-In/Test Sockets (BGA, QFN etc.)
- Memory Module Test Connectors Saw / Laser Singulation Systems
- Laser Marking / Ablation Systems
- EMI Shield Equipment
- Pick&Place Equipment
- TC / Flip Chip Bonder

- Bonding Wire (Au, Cu etc.)
- Solder Balls Wafer Bonding Systems
- C2C / C2W / W2W

- Die / Wire Bonding Tools
- Wire Bonding Capillaries
- Bonding Accessories Direct Plasma Cleaning Systems
- Batch Plasma Cleaning Systems
- Curing Ovens

- Mold Compound (green, clear)
- Mold Cleaning Material (Sheets, Pellets)
- Dicing Blades WLP Wafer Solderball Mounter
- CSP / BGA Solderball Mounter
- Laser Heater Flip Chip Bonder
- Conduction/Convection Reflow Systems
- Fluxless Reflow Oven
- Test Handling Systems
- Memory Testing Systems
- LED Prober & Sorter
- LED Die Bonder

ONTOS Equipment Systems

Booth 19

Activities

ONTOS Equipment Systems is a leading supplier of atmospheric plasma machines designed to replace vacuum equipment and wet processing to produce contamination-free, highly-activated surfaces to enhance cost, yield, and throughput in microelectronics manufacturing.
Our customers include RF, Optoelectronic and Defense market leaders. Headquartered and made in the USA with established world-wide distribution channels, sales and service is provided in more than 20 countries around the world.
Aside from other solution providers is our ability to work collaboratively with our customers to specifically tailor a system solution around their specific application and process requirements. This is achieved by continuously introducing, implementing, and integrating the latest, most advanced technology with proven robustness and reliability.

Product

▸ ONTOS Clean

The ONTOS Clean is a Standalone Semiautomated System for Surface Preparation using a patented Atmospheric Plasma with a unique design enabling without any modification using oxidizing or reducing chemistry. Ontos performs Cleaning, Eliminates the Organic Contamination, Activates Surfaces and Remove Oxidation.
An Innovative Process applies a gaseous passivation that delays the re-oxidation of the metallic surfaces.
Standard Plasma Head 25mm, 40mm, and 105mm.
Versatile Chemistry: ONTOS Clean uses Helium or Argon as the carrier gas because of their metastable energies. Customers can choose to introduce Oxygen (cleaning and activation), Hydrogen (oxide removal) or Nitrogen

▸ ONTOS IS

OEM version of the ONTOS Plasma Head for integration into third party equipment. The Plasma Curtain is available in several widths (down to 10mm) to enable optimization of the gas consumption on smaller devices or to adapt to larger devices. Integration engineering resources available.

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PacTech

Booth 15

Activities

PacTech - Packaging Technologies GmbH, established 1995 and a group company of NAGASE & CO., LTD., manufactures equipment for the microelectronic & advanced packaging industry and offers wafer level bumping & packaging contract manufacturing out of Nauen, Germany (HQ), and through the 100% subsidiaries PacTech ASIA Sdn., Bhd., Penang, Malaysia and PacTech USA Inc., Silicon Valley, USA.
Those unique and highly innovative manufacturing systems are providing solutions for today's tasks and challenges in advanced packaging applications.

Product

The equipment product line consists of solder jetting equipment (SB2-Jet), wafer-level solder ball transfer systems (Ultra-SB2), wafer-level solder rework equipment (Ultra-SB2 300 WLR), laser assisted (LAB, LCB, LAR) flip-chip bonders (Laplace) and automatic wet chemical lines for high volume electroless NiAu & NiPdAu bumping (PacLine 300 A50).
The wafer level packaging & bumping subcontractor services consist of electroless Ni/Au, Ni/Pd and Ni/Pd/Au Under Bump Metallization (UBM) for either wafer level solder bumping for Flip Chip or WLCSP or for wire bonding. Additionally, PacTech offers AOI, X-Ray, SEM, FIB, BCB Repassivation, wafer-level redistribution, wafer backside metallization, wafer thinning, laser backside marking, wafer dicing and chip singulation.

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Plasmatreat

Activities

Atmospheric Plasmatreat treatment machines are a key asset for achieving cost-effectiveness and process reliability.

- For transparent, scratch-proof coating of displays, it significantly reduces the reject rate and ensures a flawless appearance.
- When printing electrically conductive coatings on printed circuit boards, prior plasma activation, microfine cleaning ensure that the coating will adhere securely.
- In chip packaging, Openair-Plasma® microfine cleaning eliminates the need for a vacuum chamber, so process flows can be greatly simplified.
- The Openair-Plasma® process is completely potential free, it facilitates the complex process of conformal coating by extending the process window and increasing the quality of the coating.
- On cell phones and laptops, plasma pretreatment is used for VOC-free finishes ; it avoids the use of VOC's (volatile organic compounds)

Product

Plasmatreat's Openair-Plasma® cleaning and activation, along with the innovative REDOX-Tool, provide advanced solutions for oxide-free surfaces, in order to enhance adhesion, electrical performance, and overall reliability. It is possible to remove oxide layers in an inline process. This requires only a combination of nitrogen and hydrogen. This process does not need environmentally harmful formic or citric acid. Designed as a tunnel solution, the system has 3 zones: pre-heating, reduction by plasma, cooling zone. Production flexibility is provided. If required, the tool can be equipped with 2 tunnels to increase throughput. Optionally, all process-relevant data can be recorded and made available via SECS/GEM. Optional, a barcode scanner ensures the traceability.
This results in improved joint quality, better electrical and thermal conductivity, and enhanced overall reliability of the semiconductor devices. Additionally, the use of fluxless processes can simplify the manufacturing process and eliminate problem of flux residues. Using the REDOX® -Tool in TCB processes, ensures that oxide layers do not negatively affect the performance and reliability of the power module throughout the assembly process, from the DCB substrate to die attach, wire bonding, sintering and moulding.

Booth 14

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Protavic International

Booth 23

Activities

Protavic International is a French company, that designs and develops resins, adhesives and inks for the electronic industry, with operations in Europe, the United-States, South Korea and China.
Protavic International is a subsidiary of Protex International, which develops, manufactures and markets specialty chemical additives.
Protavic International offers high-value added solutions for optimized industrial processes. From the component to the final electronic card,
Protavic products glue, protect and bond in all steps of the process. It is possible to use the products as Die-Attach, Dam & Fill, Underfill, encapsulant, thermal dissipator...
Protavic International is present in many sectors such as electronics, aerospace, acoustic, automotive, medical, optoelectronic, solar energy...
Domains : Conductive and insulating adhesives, Die attach, Terminations, Dam&Fill, Glob top, Thermal dissipation, Encapsulation and Potting, Underfill, Conductive inks, Silver nanowires. Epoxy, Acrylic, PU, Polyimide, Silicone and Hybrid products.

Product

Resins and Adhesives for the electronic industry

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Roartis

Activities

Roartis stands for innovative and quality electronic adhesives, resins, coatings, inks and sinter-materials, for demanding, high reliability applications developed and produced in Europe!
Roartis' materials have been used for many years in high reliability applications and markets such as the semiconductor industry, aviation, medical, aerospace, defense, energy, automotive and industrial electronics.
With state of art laboratories and manufacturing facilities in the center of Europe, optimized and focused towards small to medium sized volume applications, Roartis is well positioned to meet the stringent requirements of the current and future electronic market requirements.
All the materials developed and commercialized by Roartis are compliant to the latest environmental regulations, such as RoHS, REACH, WEE and the End-Of-Life-Vehicles directive.

Product

Our product portfolio includes:

- Electrically conductive adhesives & sinter materials
- Insulating adhesives
- Thermally conductive adhesives
- High temperature resistant materials
- Underfills
- Glob top and Dam & Fill resins
- Liquid resins for encapsulation and potting,
- Flame retardant materials, UL94-V0 certified,
- Optically clear adhesives, coatings and encapsulants
- UV-curable adhesives & inks, for photonics packaging
- Refractive index matching materials

Booth 42

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SERMA
Microelectronics

Booth 5

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Activities

SERMA Microelectronics brings over 30 years of expertise to the table, specializing in the provision of chips and the assembly of semiconductors for industries where reliability is paramount, such as defense, aerospace, and medical sectors.
With a workforce of 90 employees as of 2023, spread across two production facilities located in Périgny (La Rochelle) and Pinsaguel (Toulouse), and boasting a clean room spanning over 1000 m², SERMA Microelectronics not only supplies and manufactures specific substrates but also assembles trustworthy products using a variety of technological components.
SERMA Microelectronics is equally involved in MCO (Maintenance in Operational Conditions) issues by maintaining proven processes and making sure they are long-lasting, as well as in the development of technological bricks that can be used to integrate more recent types of technology (MEMS, High pin count devices, MMIC, BGA, etc.), thus combining its microelectronics and SMD transfer resources in manufacturing SiPs (System In Package).
With a robust background in assembling Hi-Rel components, particularly hermetic ceramic and organic substrates, SERMA Microelectronics collaborates closely with its clients to navigate the intricacies of specific technologies and mission profiles, developing tailored integration processes to meet their exacting requirements.

Product

SERMA Microelectronics offer is subdivided in three main activities:

- The Engineering department, in charge of the development of various assembly processes in order to industrialize the customers' products. This division is also responsible of the design of organic and ceramic substrates according to the scope and the complexity.
- The Production department, which implements assembly processes. This pole also includes:
- The Die Management division which deals with active devices (procurement, sawing, visual inspection, and storage)
- The Thick Layers pole, which defines and implements inks screen- printing to produce substrates with high environmental performance.
- The Thin Film Department, which defines and produces substrates for microwave applications and high reliability photonics, using sputtering and photolithography technologies.
- The Test division, in charge of the functional verification of manufactured products through reliability and qualification sequences.

SET

Activities

Based in France, SET is a world leading supplier of high accuracy Flip-Chip Bonders excelling in high-end, demanding applications.
Since 1975, we have accompanied laboratories and industries, which look for a high precision and an important reliability in the assembly of their components. We accelerate their developments of the chips of future thanks to our robust and precise Flip-Chip Bonders.
With Flip-Chip Bonders installed worldwide, we are globally renowned for the high post-bond sub-micron accuracy and the high flexibility of our equipment. Ranging from manual loading version to fully automated version, our systems cover a wide range of applications and offer the unique ability to handle both fragile and small components onto substrates and wafers up to 300 mm.

Product description

- ACCµRA M, ± 3 µm post-bond accuracy,
- Manual Flip-Chip Bonder for universities and R&D institutes
- ACCµRA100 / OPTO, ± 0.5 µm post-bond accuracy
- Semi-automatic Flip-Chip Bonder for optoelectronics and silicon photonics
- ACCµRA Plus, ± 0.5 µm @ 3 σ post-bond accuracy
- Automatic Flip-Chip Bonder designed for production
- FC150, ± 1 µm post-bond accuracy / FC300, ± 0.3 µm post-bond accuracy
- Flip-Chip Bonders for advanced R&D and pilot line oriented
- NEO HB, ± 0.5 µm @ 3 σ post-bond accuracy
- Automatic Flip-Chip Bonder for hybrid bonding, dedicated to production

Booth 7

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SET Corporation

Synergie CAD PSC

Booth 31

Activities

SYNERGIE CAD PSC is specialized in Semiconductor IC's industrialisation and production services.
Our internal industrial capabilities located in France (Toulouse) allow to provide full back-end services from our internal supply chain in Europe/France for multiple applications (Consumer/Industrial, AI, Automotive, Space & Defence, ...), including:

- Packaging – Assembly : with our internal Packaging for small and mid series production
- Test Development and Test Production (from digital to RF-MMW)
- Reliability Qualification Laboratory
- Hardware development and fabrication (Test loadboards, Probe cards, electronic boards, ...)
- Logistics and Supply chain

For large series, our privileged partnership with Tier1 OSAT allow us to provide full TurnKey services to our customers from GDS or wafers to delivery of Finished Goods

Product

Semiconductors Back-End Engineering and Industrial services

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Taipro Engineering

Activities

Taipro offers electronic design and packaging services in microelectronics from prototyping to production. By combining its electronic know-how and microelectronics assembly capabilities, Taipro develops miniaturized electronic systems that are free of any constraints.

Technologies:

- Die placement
- Flip-chip
- Wire bonding
- Encapsulation

Booth 33

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Teledyne e2v

Booth 22

Activities

TELEDYNE e2v is developing high end semiconductor components like very high-speed data converters, edge microprocessors, and image sensors used in many markets like healthcare, life sciences, space, transportation, security and industrial markets.
Today our customers can benefit of our assembly and test capabilities, developed for very demanding markets, and based on more than 40 years 'experience and expertise in producing unique quality custom solutions to fit best with its customer's needs.

Product

Located near Grenoble (France), TELEDYNE e2v offers a one-stop-shop approach by proposing the entire assembly & test supply chain and offering fully custom solutions: substrate design, procurement, assembly, test and qualification.
Our Service proposes a wide range of assembly and test capabilities:

- Assembly: Flip-chip for die size up to 550mm² and more than 11 000 bumps, on advanced CMOS technologies; wire bond with gold or aluminum, GaAs technologies dies, System in Package and Heterogeneous SiP, Multi-Chip Module, SMD mounting on organic or ceramic substrates.
- Test: wafer probing, package testing, screening or burn-in, and qualification, digital high speed signal test, RF test, analog test data converter, microprocessors, image sensors.

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UniTemp

Activities

Thanks to our in-house development and production, our team at UniTemp is able to react quickly and with high quality to changes and changing conditions.
The continuous improvement of our devices ensures that we are as close as possible to our customers' requirements.
This is why each of our appliances also offers a wide range of different options and upgrades.
For 24 years, UniTemp has been active in the field of reflow solder furnaces as well as RTP annealing systems. We specialize in equipment for thermal processes.
We mainly supply customers in the R&D sector for the evaluation of semiconductor and other processes.
Our target group are institutes, universities and the development departments of semiconductor manufacturers.
We are located in Bavaria close to Munich.

Product

Reflow solder ovens: We provide reflow solder systems which enable flux-less, lead and void free soldering, encapsulation of housings, soldering of power devices and solder bump reflowing.
Semiautomatic wire bonders: Our wire bonders have 3 motorized axes with an accuracy of 1,0 µm. They come with a fine table motion and provide as well deep access bonding. They can be served with gold and aluminum wires.
High precision hot plates: Our high precision hot plates are temperature controlled via a digital target and actual value display including a overheating protection. The substrates are fixed by vacuum.

Booth 1

UNITEMP
Universal Temperature Processes

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Valtronic

Booth 3

Activities

Valtronic's expertise is driving disruption in the Medtech, Diagnostics, and Advanced industrial markets.

Mission

- We provide high-quality turnkey solutions that facilitate technological disruption
- We push industrial technologies to their limits
- We provide professional project management from design to manufacturing
- Our customers benefit from best time-to-market
- Values
- Customer satisfaction
- Excellence through individual responsibility
- Mutual respect and constructive attitude
- Commitment to integrity and ethical business

Product

▸ **Innovative Assembly Processes**

Valtronic's facilities are equipped with first-rate SMT and microelectronics technologies to address all your assembly needs for innovative industrial, medical and diagnostics devices.

Our capabilities include:

▸ **Printed Circuit Board / Substrates**

- Multi-layer / High Density Interconnect (HDI) PCBs, Rigid, Flex & Rigid-Flex
- Copper Tracks down to 15 microns, Thickness : min. 25 microns
- Pitch: min. 30 microns (Copper Pillar)

▸ **Combined Assembly Technologies**

- SMT, micro SMT (008004), CoB (Chip on Board), FC (Flip-Chip)
- BGA with multi-die, CoC (Chip on chip), CSP (Chip Scale Package)
- MCM (Multi-Component Modules)
- Board wash, Soldered Flip-Chip of micro BGA
- Conformal Coating Automatic Dispensing, Underfill Automatic Dispensing

▸ **Manual Assembly**

Our manual assembly technicians have been developing their skills for over fourty years. They assemble your most challenging parts with discipline and goldsmith's precision. This proficiency, originating from the Swiss watch valley, has been extended to all of the Valtronic sites. Additionally, your product costs can be optimized through partial or full assembly of your device in Valtronic's Moroccan facility.

▸ **Clean Room Assembly**

Our manufacturing facilities are equipped with clean rooms compliant to the ISO 5 and 7. Our customers benefit from a dedicated clean room area for the assembly of highly sensitive devices such as Class III implants.

▸ **Design for Manufacturing**

With our expertise, we are able to develop PCBs while anticipating the production process and considering all possible obstacles related to mass production

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Yole Group

Booth 48

Activities

Yole Group is an international company recognized for its expertise in the analysis of markets, technological developments, and supply chains, as well as the strategies of leading players in the semiconductor, photonics, and electronics sectors.
With a relationship of trust established over the years, Yole Group maintains regular interactions with these leading companies, aiming to share and exchange its vision of markets and technologies.
Driven by committed and curious individuals, Yole Group benefits from this sharp expertise at the intersection of markets and technologies in the semiconductor industry, enabling it to offer a comprehensive and unique vision of the sector.
More information is available on the company's website: www.yolegroup.com.

Product

With a team of over 180 people worldwide, Yole Group publishes market, technology, performance, reverse engineering, and cost analyses from More than Moore to More Moore technologies and markets. The company also offers strategic marketing consulting and technological analysis services.
Yole Group operates through two distinct brands:

- • Yole Intelligence, which specializes in market analysis, technological advancements, and strategic insights of major industry players.
- • Yole SystemPlus, which concentrates on analyzing technologies, technical decisions of industry leaders, and examining manufacturing costs of systems and components.

With a team combining market, technical, and financial expertise, Yole Group also develops consulting activities related to mergers, acquisitions, and business valuation.

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Yole Group

Call for Abstracts: THERMAL 2026

19th Advanced Technology Workshop on Micropackaging and Thermal Management
La Rochelle, France **March 25th – 26th 2026**

We are pleased to open the call for papers of the 19th Advanced Technology Workshop on Micropackaging and Thermal Management that will be held in **La Rochelle** on **March 25th and 26th, 2026**. This yearly conference has grown year after year by the number of presented papers and attendees.

Be part of a successful 2026 edition and be sure to submit your abstract on time. The workshop sessions will include the following topics. Papers are invited in following areas:

- Cooling solutions for microelectronics packaging,
- Heat conductive materials at chip, board, sub-system and system levels,
- Advances in PCBs for thermal management, PCB embedded components included,
- Heatsinks, heat pipes and change phase materials,
- Liquid and phase change cooling,
- Thermal modeling and simulation, Machine Learning and AI optimization,
- Innovative cooling solutions,
- Thermal management of optoelectronics components (LEDs, IR sensors...),
- Overviews or examples of products, systems cooling, power electronics, automotive transport,
- Temperature-related or thermal cycles-related reliability of electronic components.

Speakers will submit 200-300 words abstract detailing their presentation (20 minutes + 5 minutes for questions), no later than **10th, January 2026**.

Speakers pay a reduced registration fee (including MERCURE hotel accommodation for 2 nights and meals) and are also requested to attend the entire workshop to maximize opportunities of exchanging with other attendees and exhibitors.

Notification of acceptance by the Technical Committee: 20th, January 2026. After notification of acceptance, you commit to attend the workshop or delegate someone else.

Please respond to imaps.france@orange.fr

▸ **Conference Chairmen**
Jean-Yves Soulier (Safran Data Systems)
Bruno Levrier (Bruno Levrier Expertises)
Jean-Pierre Fradin (ICAM Toulouse)

▸ **Technical Program Committee**
Mohamad Abo Ras (Berliner Nanotest)
Boguslaw Wiecek (Technical University Of Lodz)
Dave Saums (Ds & A Llc)
Thomas Harder (Ecpe)
Raphaël Sommet (Xlim Université de Limoges)
Sandrine Feneyrou (Safran Data Systems)
Vincent Ayel (CNRS-ISAE ENSMA-Université de Poitiers)

Call for Abstracts: ESTC 2026

11th IEEE Electronics System-Integration Technology Conference
Helsinki, Finland **September 9–11, 2026**

The 11th IEEE Electronics System-Integration Technology Conference (IEEE ESTC) is the leading international forum for electronics packaging and system integration. The conference is organized every two years in Europe and is supported by IEEE-EPS in association with IMAPS Europe. Join us to explore the latest advancements and insights from experts across the field. In addition to the technical program, IEEE ESTC will also feature an exhibition showcasing the latest products, technologies, and solutions from industry leaders.

Don't miss this opportunity – save the date today!

Abstract submission opens on **December 1, 2025**. We invite authors to submit abstracts on the following topics, among others:

- Advanced Packaging
- Materials for Interconnects and Packaging
- Optoelectronic Systems Packaging
- Assembly and Manufacturing Technologies
- Design Tools and Modeling
- Power Electronics System Packaging

We look forward to your contributions and to welcoming you at IEEE ESTC 2026!

▸ **General Chair:**
Toni Mattila,
Business Finland, Finland
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EMPC 2027

The 26th European Microelectronics and Packaging Conference (EMPC) & Exhibition
Ingolstadt, Germany **September 14-16, 2027**

The European Microelectronics and Packaging Conference (EMPC 2027) is the premier international conference for microelectronics packaging, owned and sponsored by IMAPS-Europe and co-sponsored by IEEE-EPS. The event brings together researchers, innovators, technologists, and business and marketing managers with a shared interest in semiconductor packaging. The program will focus on both current industrial needs and trends, as well as on long-term academic solutions such as:

- Advanced Packaging & System-Integration
- Materials and Processes
- Design, Modelling and Reliability
- Markets and Developments

In addition to the technical sessions, EMPC will feature a comprehensive exhibition, offering companies and institutions the opportunity to present their latest products, technologies, and services. This exhibition provides an ideal platform for networking, business development, and discovering cutting-edge solutions in microelectronics packaging.

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IMAPS France Chapter
International Microelectronics Assembly Packaging Society

IMAPS-France (French chapter) is a non-profit organization with 200 members in 2025 from 110 companies or institutes in France and neighbouring countries (Belgium, Switzerland, Morocco, Spain, Portugal). IMAPS-France is one out of the 30 IMAPS chapters throughout the World.Our mission is to promote and to disseminate knowledge and know-how related to the packaging and assembly of semiconductor devices.

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☐ 100 € Individual member
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Organizer

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IMAPS - International Microelectronics Assembly and Packaging Society - is a global community of microelectronic related engineers, scientists, manufacturers, end-users and supply chain companies. The Society aims to support the development and growth of the Microelectronics and related industries, and to aid the transfer of knowledge and information. This is achieved through networking, seminars, workshops, short courses, publications, webinars and websites.
Members benefit from access to business networking and events at a reduced rate; technical information & receive society newsletters and other publications. IMAPS is the largest Microelectronic Packaging Society in the World !
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To that end, we organize events each year, in English language, these are namely: MiNaPAD, POWER, THERMAL and EMPC 2025 a European Event.

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26th Nov. 2026

From Nano to Macro

Power Electronics and Packaging European Workshop

GREMAN – Polytech Tours
Amphithéâtre du Département électronique et énergie
7 avenue Marcel Dassault
37000 Tours - France

Organized by IMAPS France – International Microelectronics Assembly and Packaging Society
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March 25th – 26th 2026
La Rochelle
France

Mercure Océanide
Vieux Port Sud

19th European Advanced Technology Workshop on Micropackaging and Thermal Management

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