Tuesday May 26th

Afternoon: 15.30 to 17.30 – ***Lecture BERNABE Stéphane (Project Leader – Photonic Circuits and Modules, CEA-LETI) Makalu Room***

Wednesday May 27th

8h45 Welcome to MINaPAD

9h00 Opening by Alexandre Val (Auditorium)

9h30 Keynote 1: Jonathan Abela (UTAC) - Capturing Value in the Automotive Market Technology Race (Auditorium)

10h15 – 10h40 Exhibition Opening (Exhibition Hall) / coffee break sponsored by

SESSION A:
Hi-Rel Packaging 1

10h45 High integration GaN power module
(#29, CEA LETI)

11h10 Mid-power and high efficiency package – aEASI, die embedded in leadframe
(J-M YANNOU, ASE Group, Taiwan)

11h35 Impact of Package and PCB Features on the Reliability of Solder Joints in GaN Packages
(P. HAGHPARAST, Université de Sherbrooke, Canada)

12h00 – 13h10 Lunch (Exhibition Hall)

	SESSION B: Modeling & Simulation	SESSION C: Material, Process, Manufacturing
13h15	A novel approach of optimal of step-stress accelerated degradation test plan (M-T TRUONG, CEA LETI, France)	New Solutions for plasma dicing, SiC wafer processing and residue free wafer surface protection film (G. KLUG, DISCO, Germany)
13h45	Assessment of moisture impact on 3D integrated stack (V. CARTAILLER IMS/STMicroelectronics, France)	Plasma Cleaning Technology for Microelectronics Assembly Process (R. FURUKAWA, PANASONIC, Japan)
14h15	Numerical and Experimental Study on Thermomechanical Stress in a 3D BSI Image Sensor stacked by Cu/SiO2 hybrid Bonding (C. SART, STMicroelectronics, France)	Ultra-thin base materials take PCB miniaturization to the next level (D. SCHULTZE, DYCONEX, Switzerland)
14h45	Impact of the assembly process on the mechanical behavior of integrated circuit packages. Application on FCBGA package (Y. BOUTALEB, STMicroelectronics, France)	A New halogen-free vapor phase organic coating for high reliability & protection of miniaturized and dense electronics in harsh environments (R. KUMAR, SPS, USA)

15h15 – 15h40 Exhibition / Coffee break sponsored by

	SESSION D: Process Optimization	SESSION E: Opto Electronic
15h40	Fine Copper Wire Bonding-Solution to solve Defectivity (J. CATANIA, STMicroelectronics, France)	Innovative curved micro display packaging for lightweight augmented reality headset (F. ZUBER, CEA LETI, France)
16h10	Active Mold Packaging for novel CSP leadframe designs and bond-less die to leadframe interconnects (F. ROICK, LPKF, Germany)	PIXCURVE: an innovative approach using standard packaging for curved optical components (D. HENRY, CEA LETI, France)
16h40	Conductive glue screening for die attach on gold surface in BGA/LGA packages (F de MORO, STMicroelectronics, France)	Residual stress in CdHgTe infrared detectors induced by fabrication and use at 100 K Impact on mechanical properties and reliability (R. PESCI, ENSAM, France)

SESSION F: Characterization

17h10	Evolution of SAC solder's plasticity characteristic under thermal cycling and its effect on reliability predictions (G. KHOURY, IMS, France)
17h40	New algorithm for in-situ 3D CTE calculation: application for electronic and semiconductor (D. ECOIFFIER, INSIDIX, France)
18h10	Combined x-ray nano-tomography and Small Angle Neutron Scattering characterization applied to reliability and process optimization (R. Della GIUSTINA, ILL Grenoble, France)

18h40-18h50 Exhibition – End of first day

19h45 Social Event Restaurant “L’Epicurien”

Sponsored by

Thursday May 28th

8h30 ***Keynote 2: Michel Garnier, ST Microelectronics - Packaging (Auditorium)***

	Session G: Flip Chip Process	Session H: Hi-Rel Packaging 2
9h30	Copper Pillars manufacturing for advanced packaging and innovation flip chip structures (A. AIT MANI, CEA LETI, France)	Active Interposer Technology for chipset (#28 CEA LETI, France)
10h00	Low Cost Au-Stud Bump Flip-Chip Process Applicable for RF Packaging for Prototyping (M. YAZICI, Sabancy University Orta, Turkey)	From Column manufacturing to column assembly on LGA or Re-assembly on used LGA (W. AKLAMAVO, SERMA Technologies, France)
10h30	Die to wafer Hybrid Bonding Equipment: throughput versus Precision (P. METZGER, SET, France)	Influence of grain morphologies and anisotropic properties on the stress state of BGA solder joints (E. Ben ROMDHANE, IMS, France)
11h00	Assembly of very fine pitches Infrared local plane array with indium micro bumps (O. MAILLIART, CEA LETI, France)	Mechanical and thermal investigation of a novel intermetallic insertion bonding for 3D Stack (M. LOFRANO, IMEC, Belgium)

11h30-12h00 Animation Lottery sponsored by CEA LETI

12h00– 13h00 Lunch & Exhibition (Exhibition hall)

13h10 ***Keynote 3: Overview on Printed Electronics (Michel POPOVIC, president of AFELIM)***

Session I: Printed Electronics

13h40 Structured Printed Electronics (#33 CEA LETI, France)

Session J: WLP / Fan In Fan Out

14h10 Anhydride Free and Low Warpage Encapsulation for Wafer level Packaging (R. de WIT, HENKEL, Netherlands)

14h40 Fan Out wafer level package – Different flavors for different needs (C. ZINCK, ASE Group, Taiwan)

15h10 Wafer Level Integration of thin silicon dies (#31 CEA LETI, France)

15h45-15h50 Closing by Alexandre Val (Auditorium)

15h50 -16h30 Exhibition /Coffee Break

16h30 End of MiNaPAD 2020